ECE606: Solid State Devices
Lecture 37: Nonideal Effects in MOSFET

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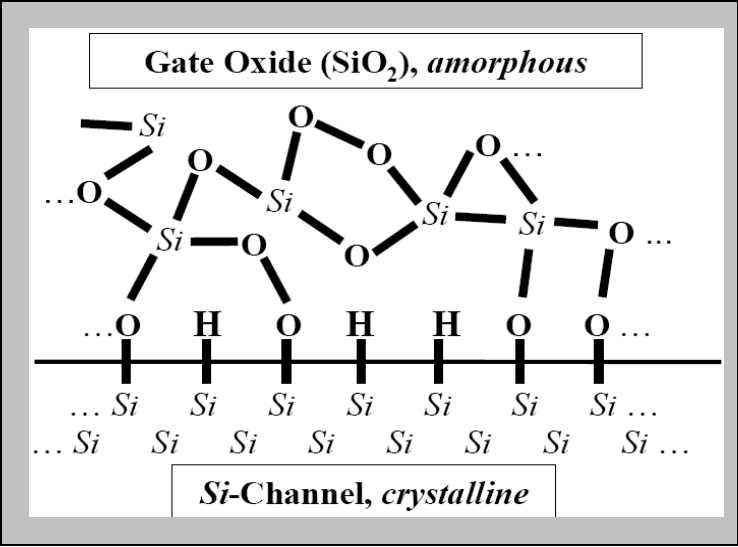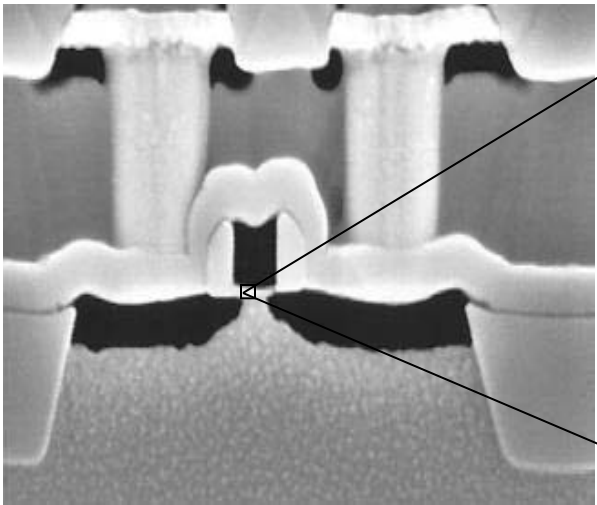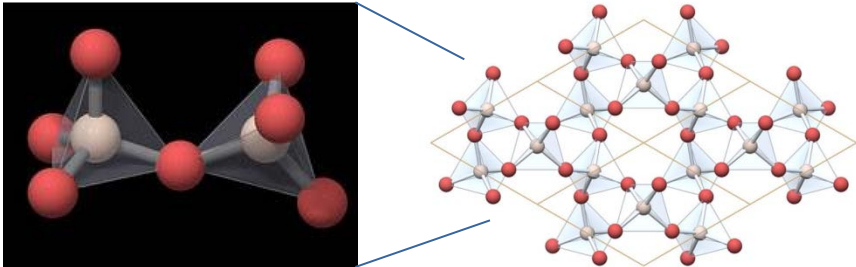alam@purdue.edu

ECE-60

Outline

1. Flat band voltage

2. VT-shift due to trapped charges
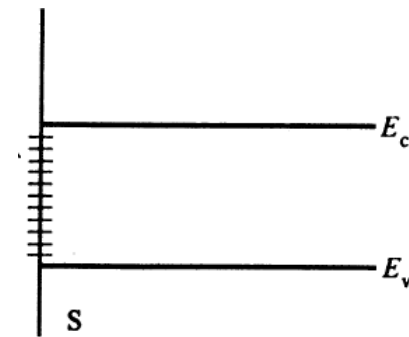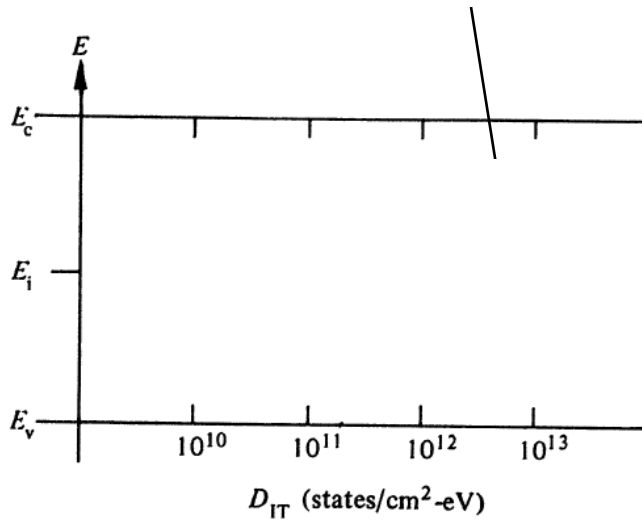
3. **Physics of interface traps**

4. Conclusion

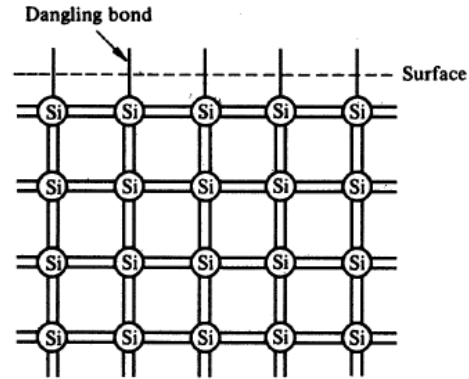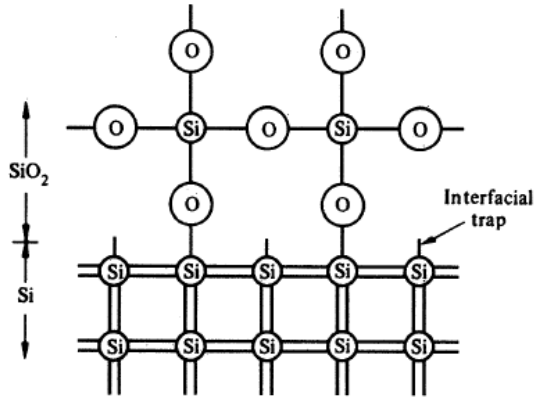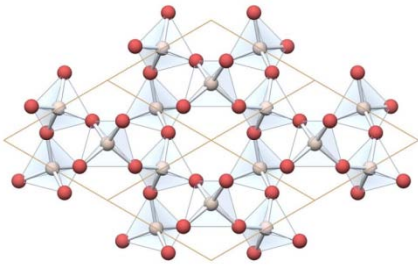$$V_{th} = V_{th,ideal} + \phi_{MS} - \frac{\gamma_M Q_M}{C_O} - \frac{Q_F}{C_O} - \frac{Q_{IT}(\phi_s)}{C_O}$$
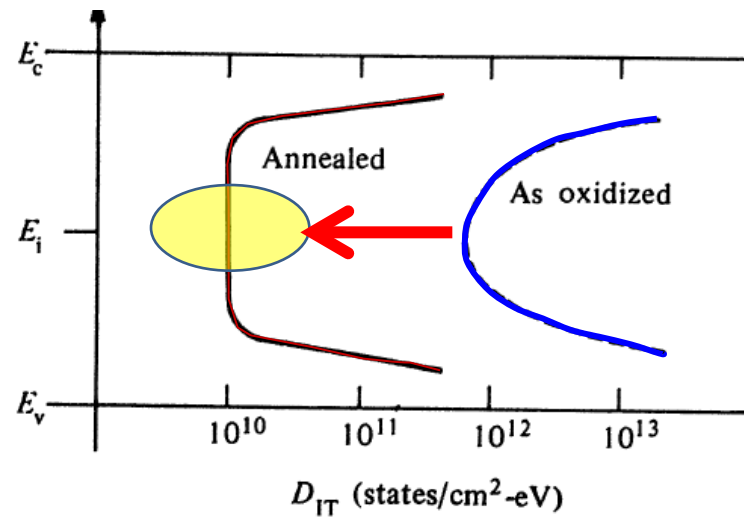
SiO and SiH Bonds

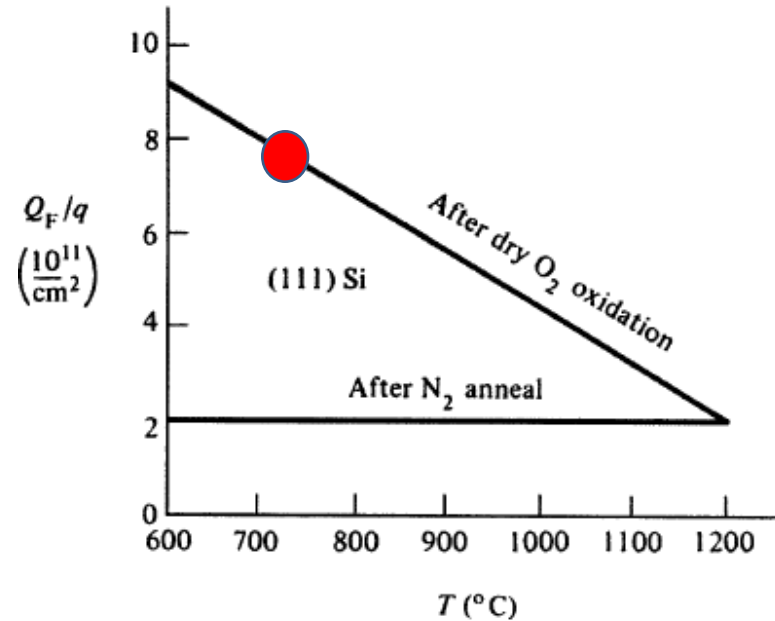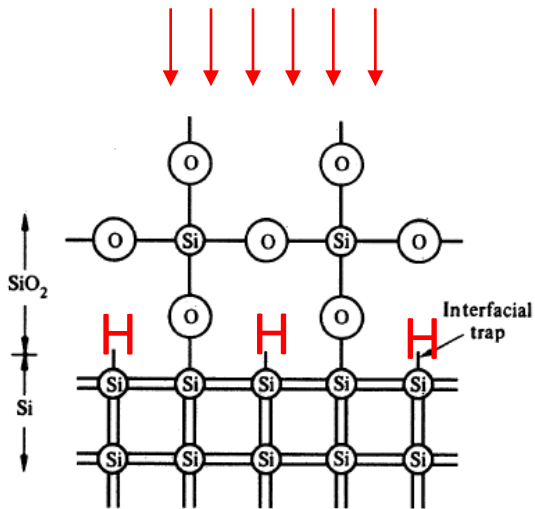Gate Oxide (SiO_2), *amorphous*

Si-Channel, *crystalline*

Interface States
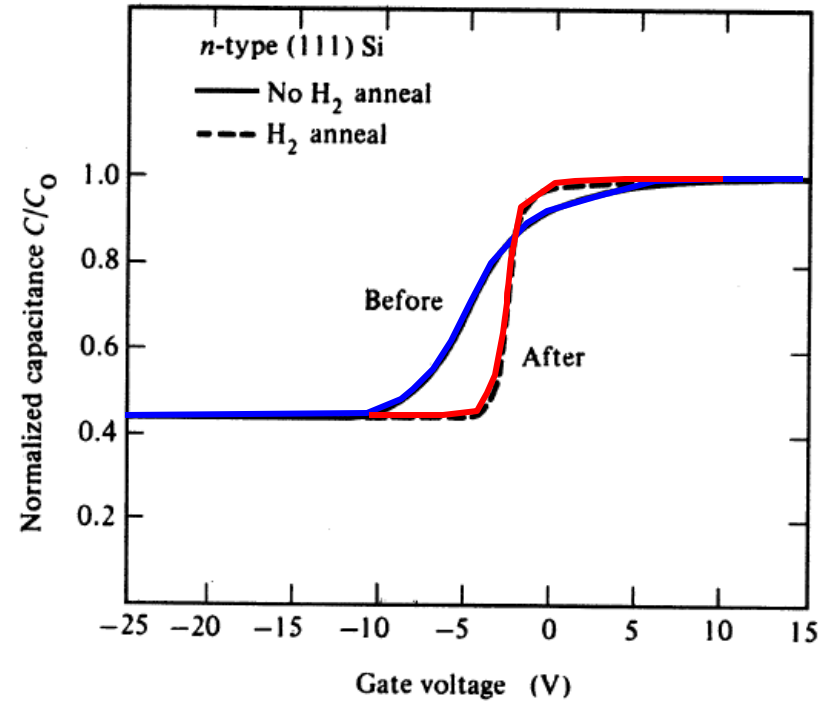

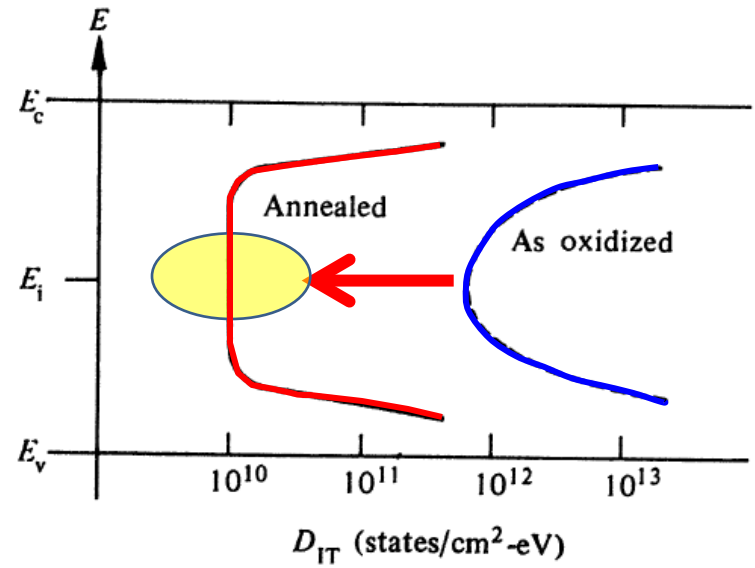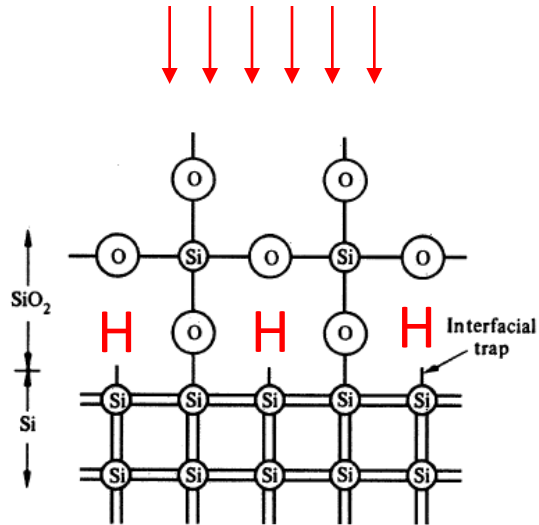HW: Unpassivated bonds ~10^{14} cm^{-2}

'Annealing' of Interface States

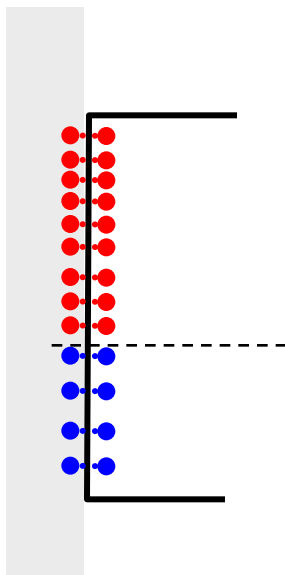**Forming gas anneal**

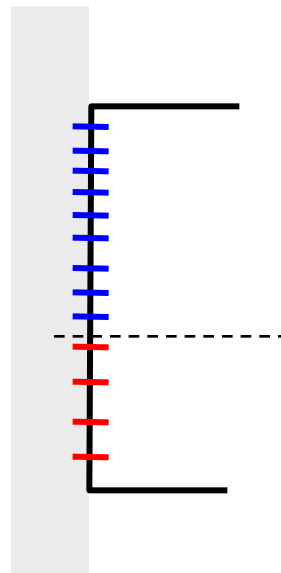# C-V Stretch Out

Forming gas anneal

Nature of Donor and Acceptor Traps

Donor level
Positive when empty
Neutral when full
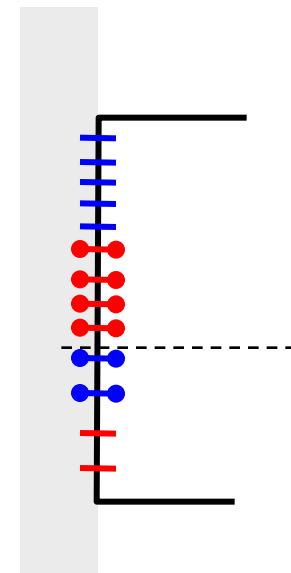
Acceptor level
Neutral when empty
Negative when full

Combination when both are present

Donor like Interface States

$$V_{th} = V_{th}^* - \frac{1}{C_{ox}x_0} \int_0^{x_0} x \times \alpha(V_G) \times Q_{ox}(x)\delta(x - x_o)dx = V_{th}^* - \frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$

$\alpha(V_G) = 0$

$0 < \alpha(V_G) < 1$

$\alpha(V_G) \sim 1$

E_c

E_F

E_v

C/C_{ox}

V_G
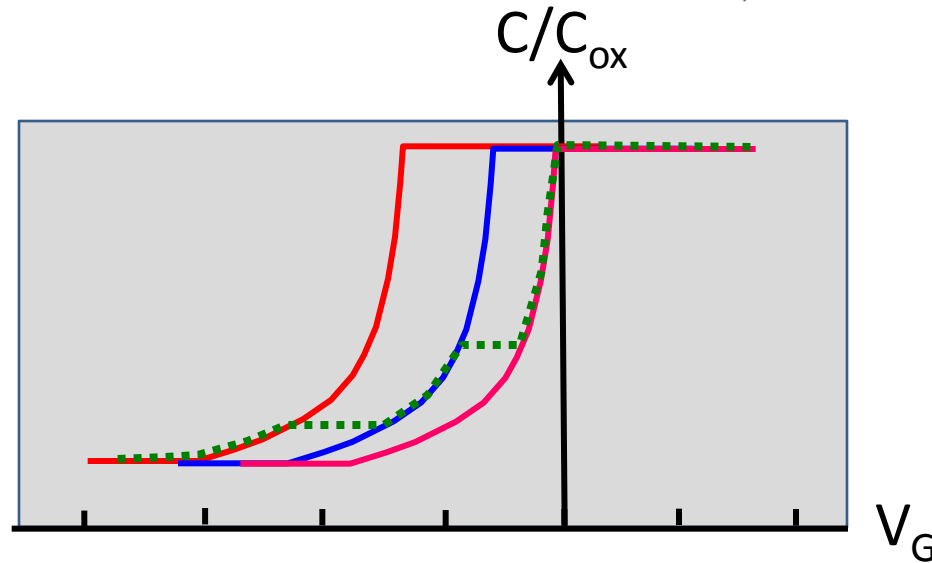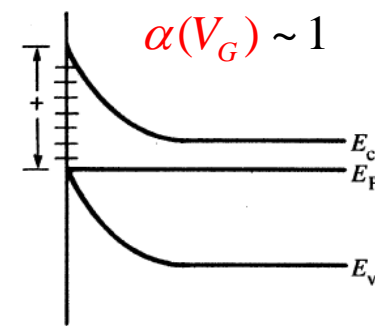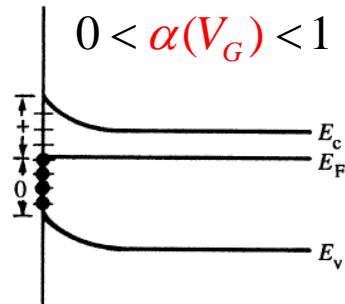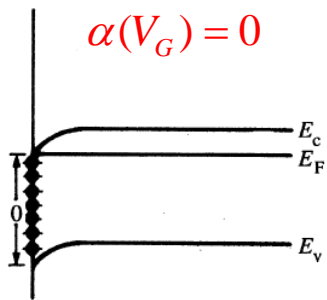
Acceptor like Interface States

$\alpha(V_G) = 0$ $0 < \alpha(V_G) < 1$ $\alpha(V_G) \sim 1$
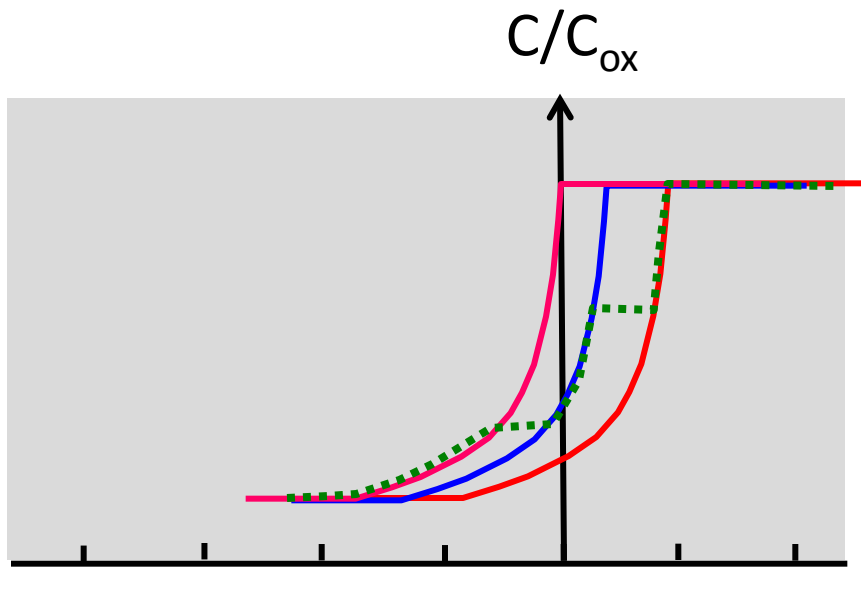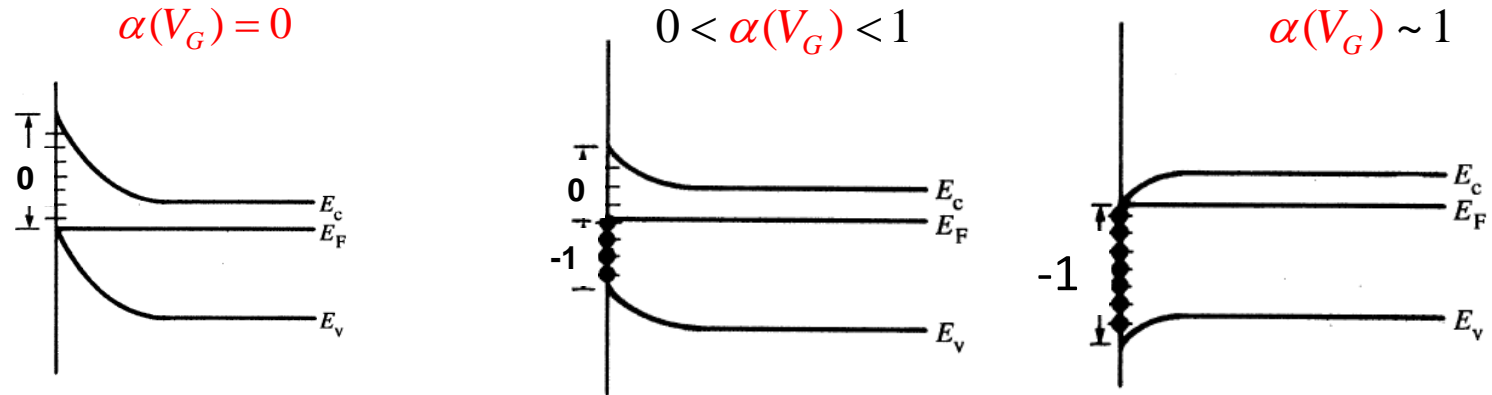
$$V_{th}(V_G) = V_{th}^* + \frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$

Acceptor and Donor Traps Combined

Donor-related stretchout

Acceptor-related stretchout

C/C_{ox}

V_G

n-type (111) Si

—— No H_2 anneal

- - - H_2 anneal

Before

After

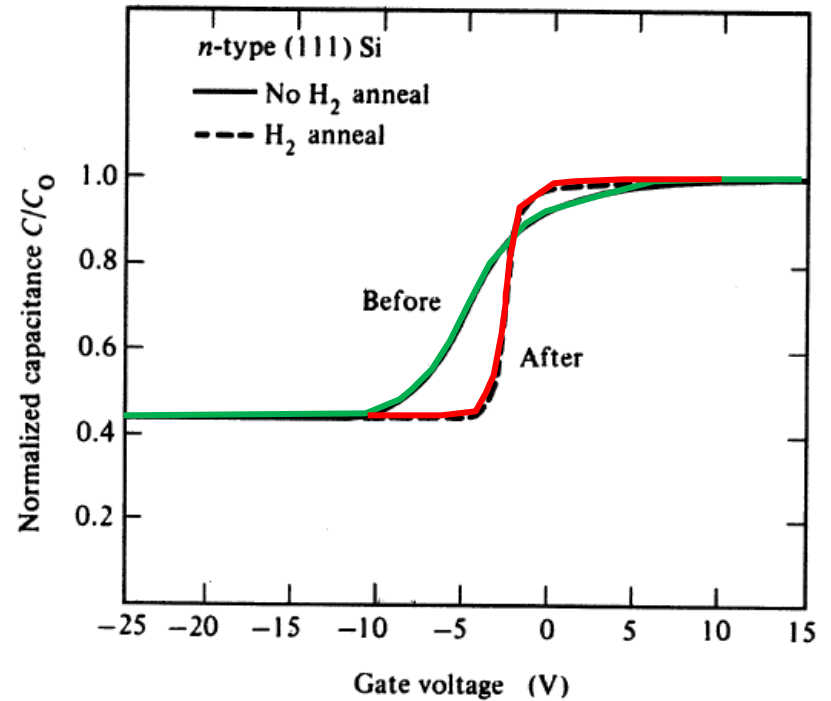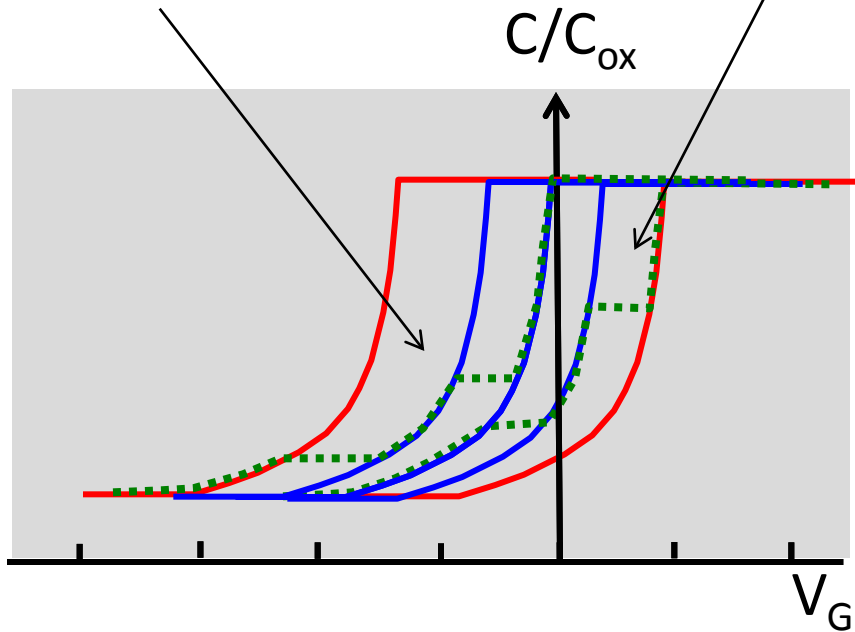Normalized capacitance C/C_O

Gate voltage (V)

Conclusion

1) Non-ideal threshold characteristics are important consideration of MOSFET design.

2) The non-idealities arise from differences in gate and substrate work function, trapped charges, interface states.

3) Although nonindeal effects often arise from transistor degradation, there are many cases where these effects can be used to enhance desirable characteristics.