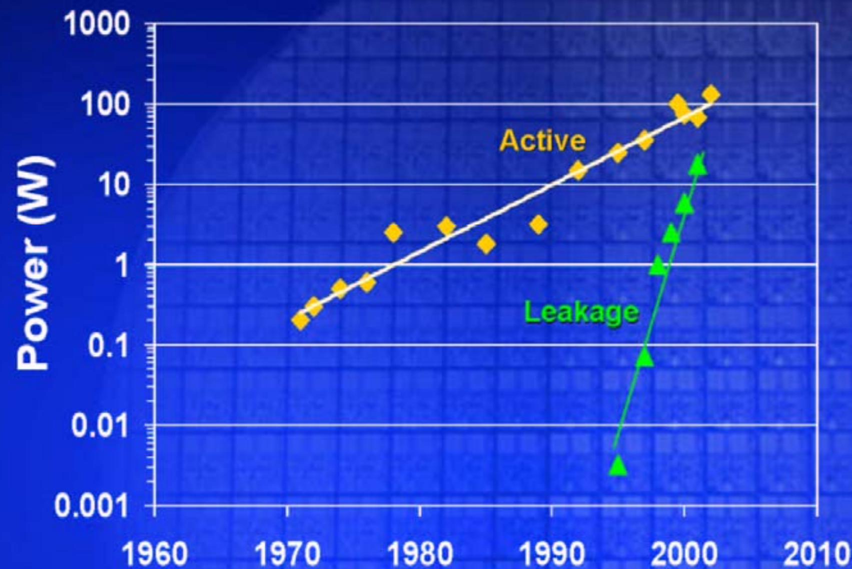
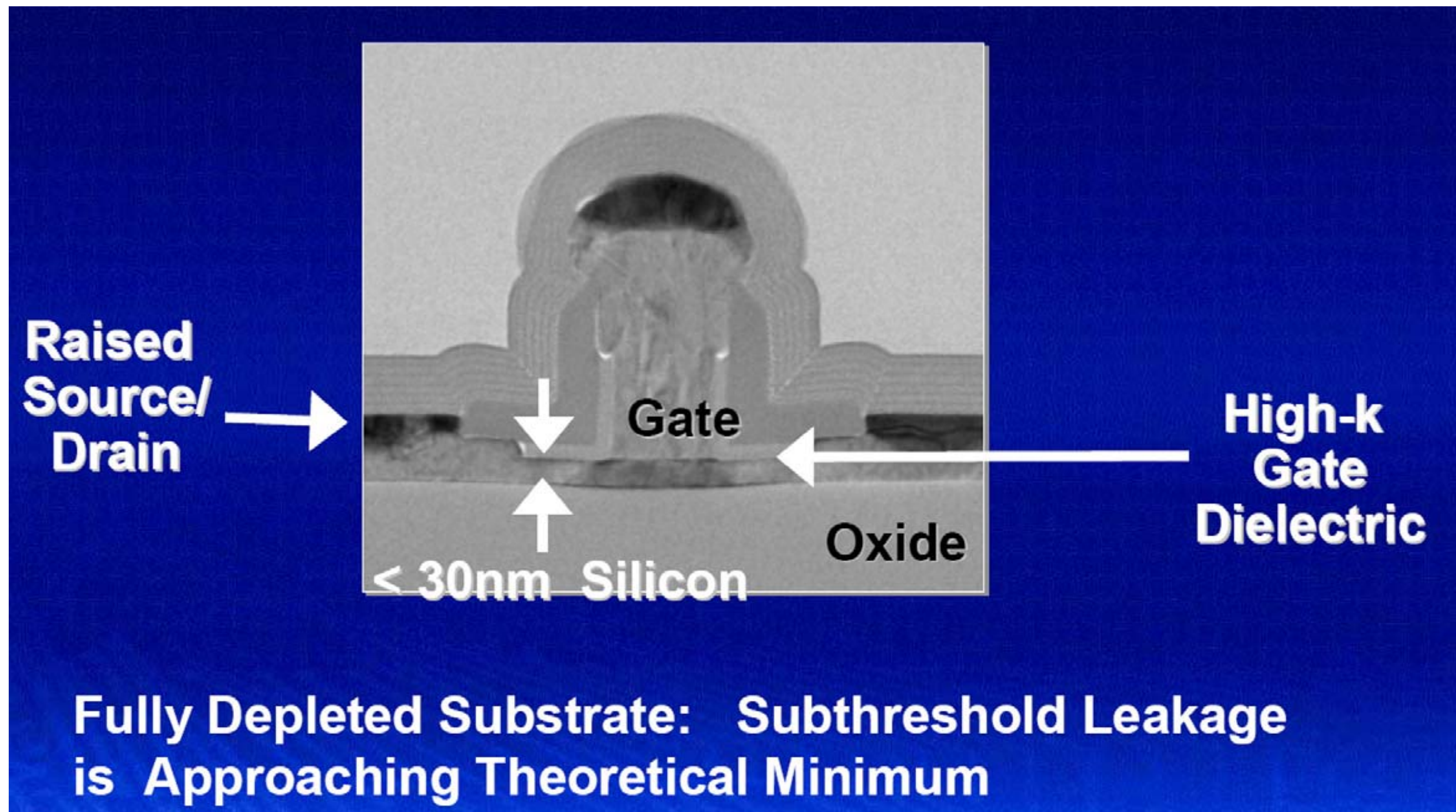
Nanomaterials

Lecture 13: Nanoscale CMOS



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

Silicon-on-Insulator (SOI) Technology



G. Marcyk, "High performance non-planar tri-gate transistor architecture," Sept. 17, 2002.

Limitations of CMOS at the Nanoscale

(7) Operating speed

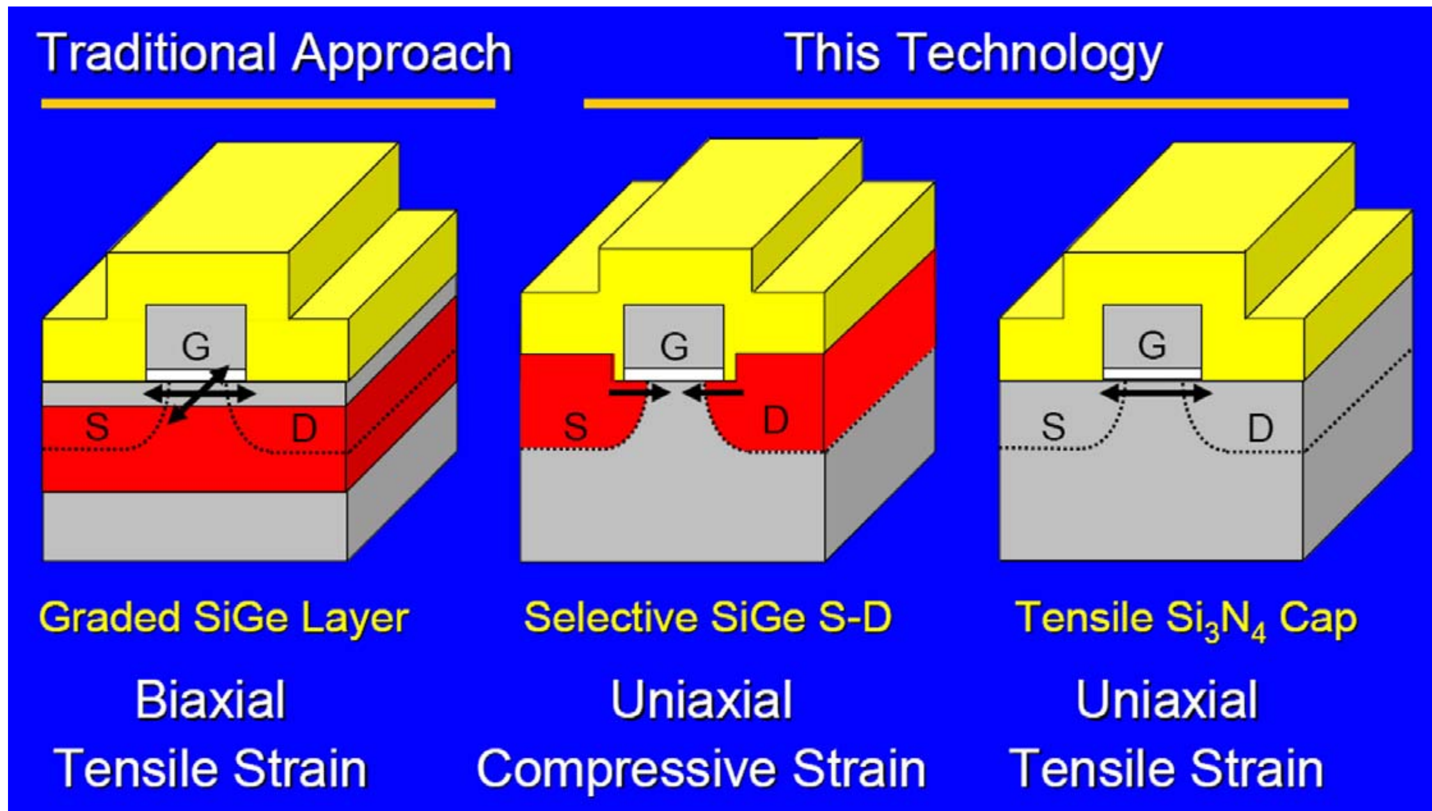
→ Speed is limited by charging time (i.e., *RC* time constant).

→ Low-k minimizes *C* and copper minimizes *R* for interconnects.

→ Transistor speed is limited by carrier mobility

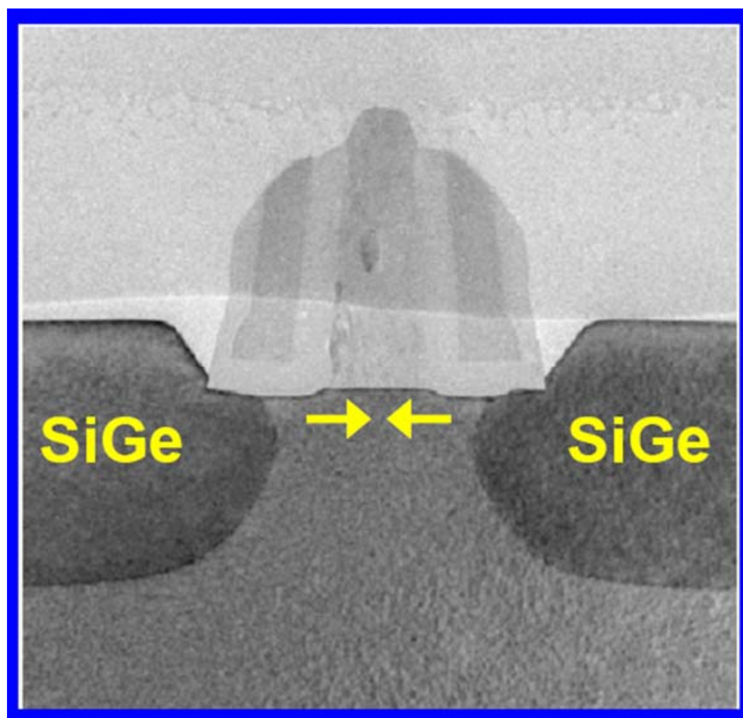
→ Carrier mobility is enhanced by intentionally introducing strain into the channel.

Transistor Strain Technologies



T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

PMOS Strain Technology: Enhancing Hole Mobility Through Uniaxial Compressive Strain

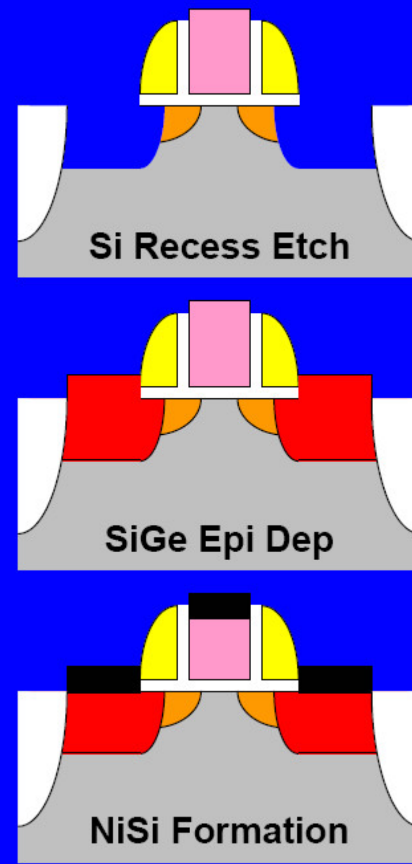


Embedded geometry + compressive source/drain = Large uniaxial compressive strain

T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

Strained PMOS Process Flow

- SiGe introduced late in the process flow → source-drain
- Si Recess Etch + SiGe Epi deposition inserted post spacer formation to standard non-strained process
- Ease of implementation



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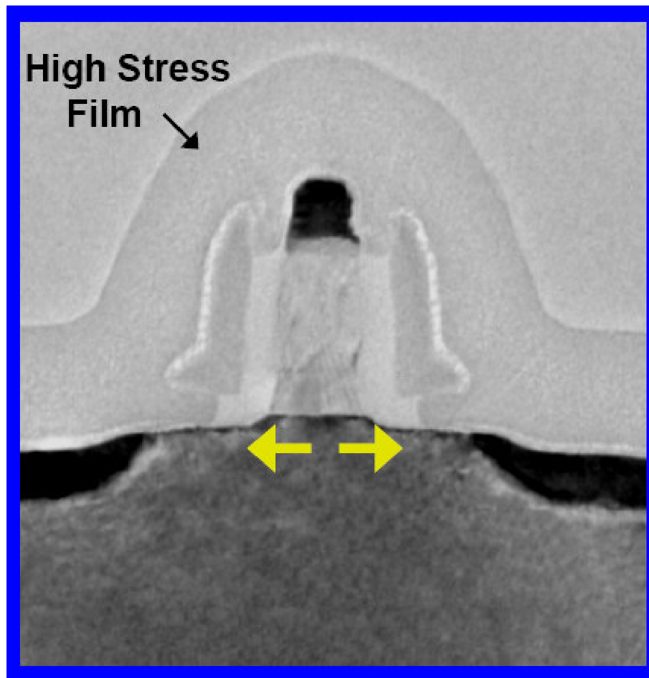
NMOS Strain Technology: Enhancing Electron Mobility Through Uniaxial Tensile Strain



Highly tensile silicon nitride capping film

T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

Limitations of CMOS at the Nanoscale

(8) Cost

→ Revenues increase by 16%/year

→ Factory cost increases by 19%/year

→ Plus, advanced lithographies (e-beam, ion beam, X-ray, EUV) are currently more expensive than DUV lithography

→ Costs are expected to rise more quickly than revenues in the future

"Moore's Law" for CMOS Economics

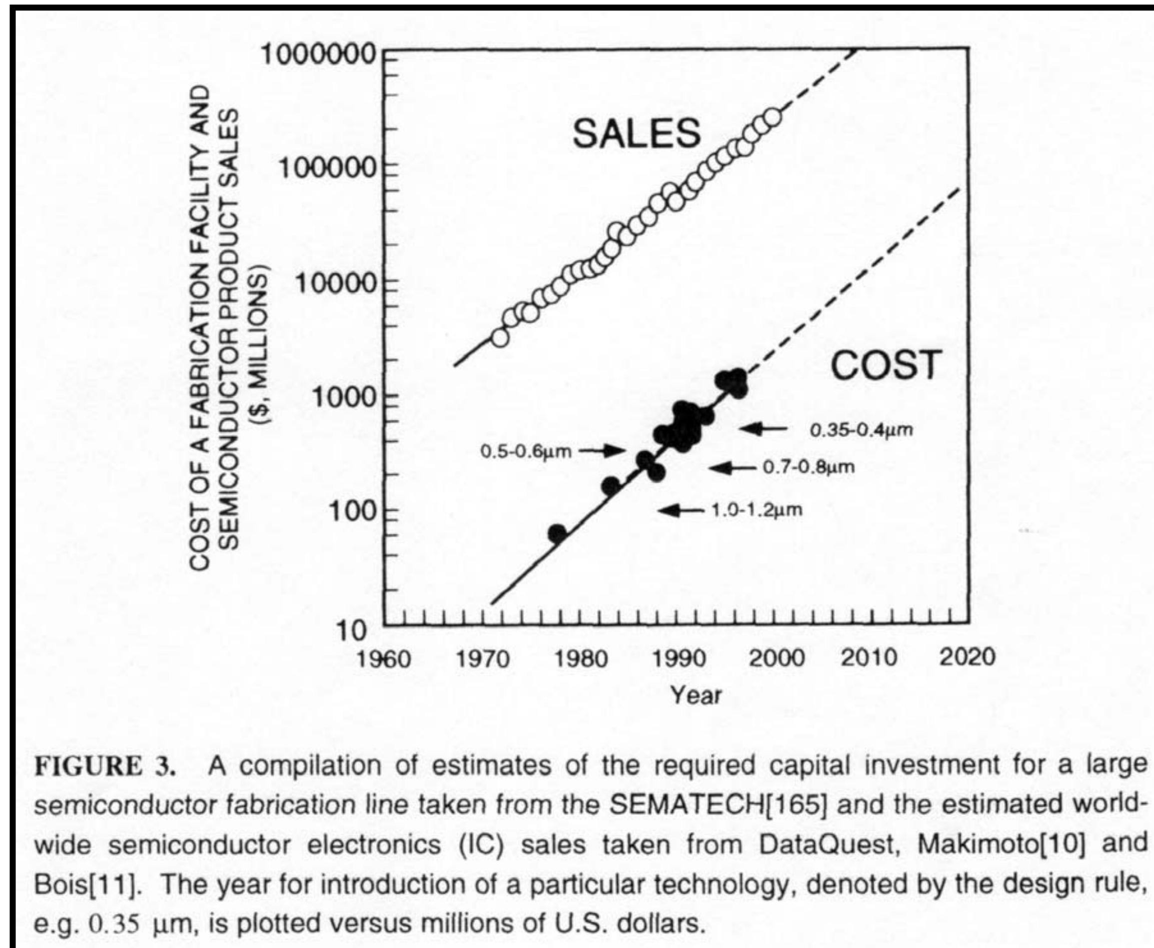
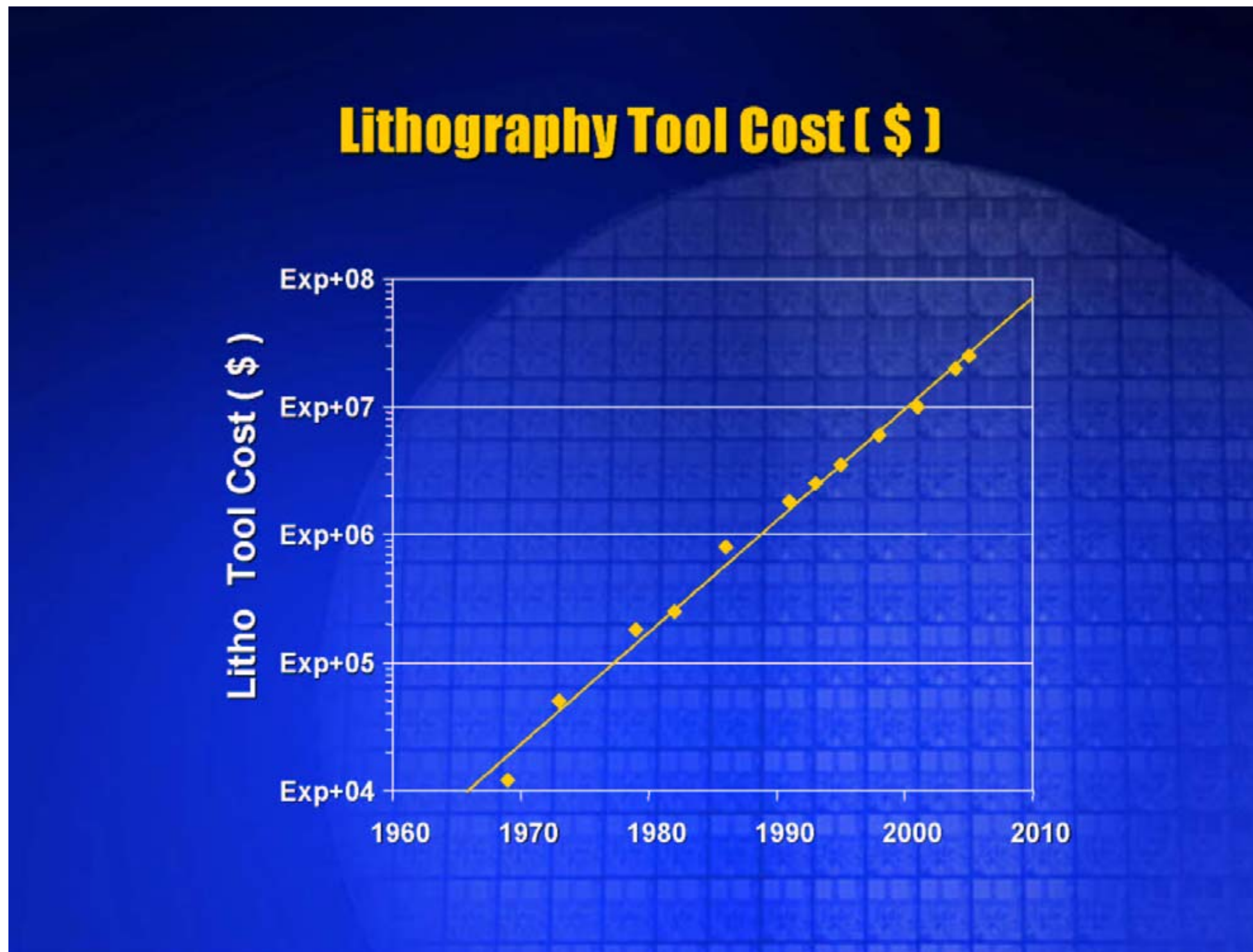


FIGURE 3. A compilation of estimates of the required capital investment for a large semiconductor fabrication line taken from the SEMATECH[165] and the estimated world-wide semiconductor electronics (IC) sales taken from DataQuest, Makimoto[10] and Bois[11]. The year for introduction of a particular technology, denoted by the design rule, e.g. 0.35 μm, is plotted versus millions of U.S. dollars.



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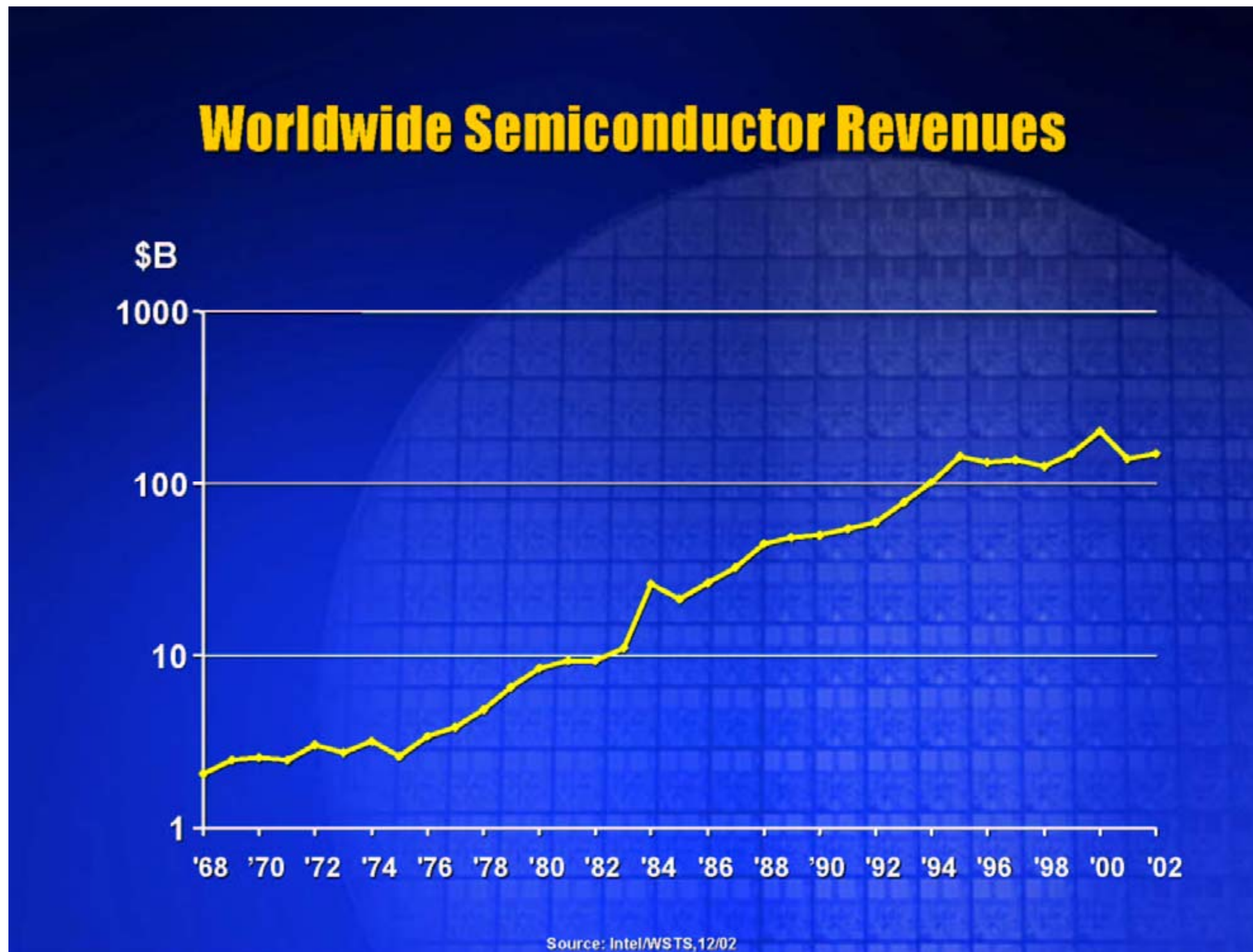

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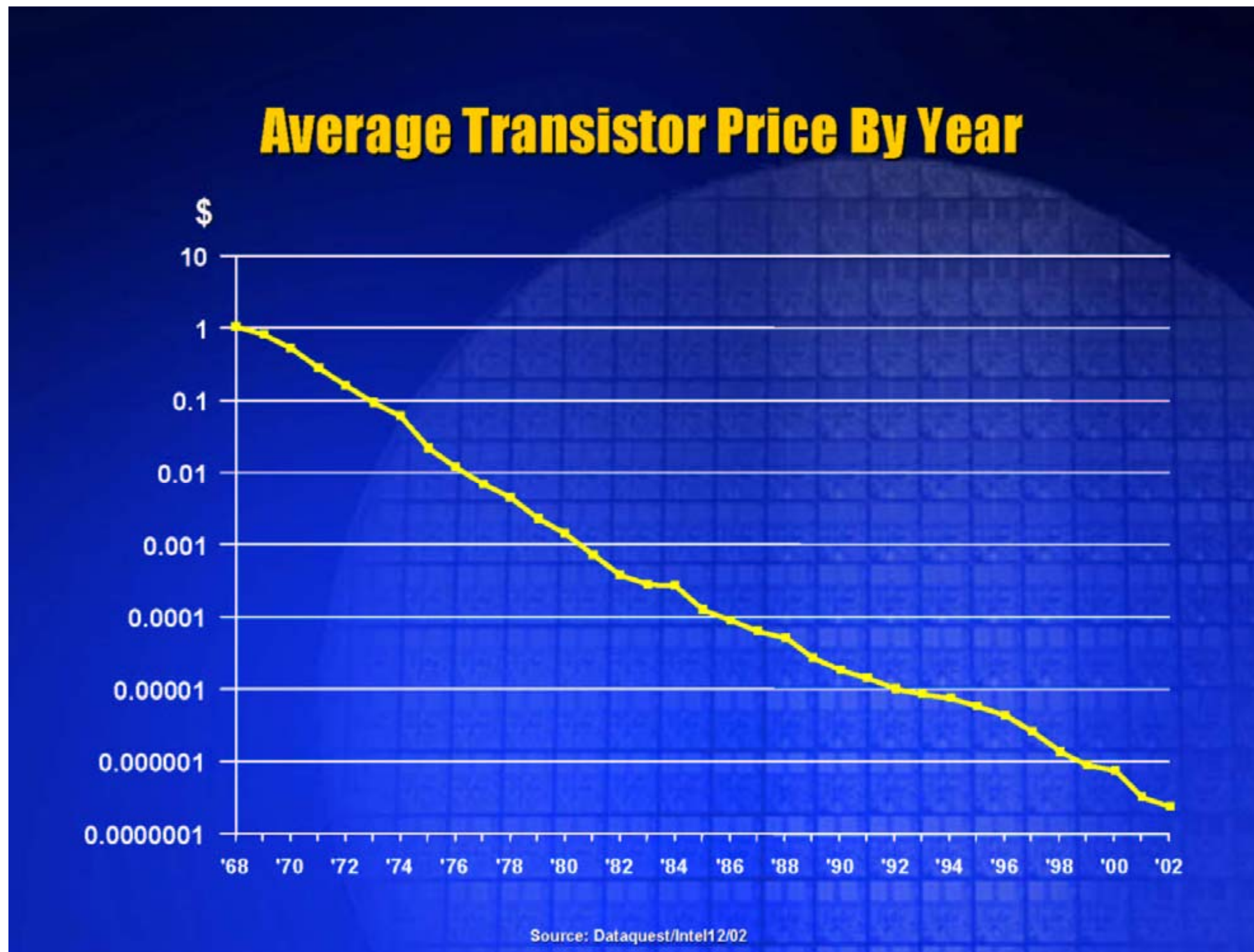

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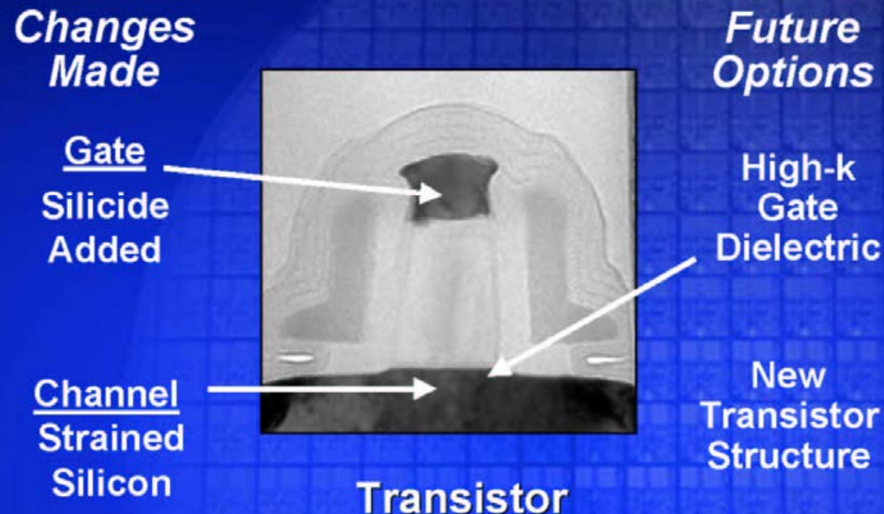

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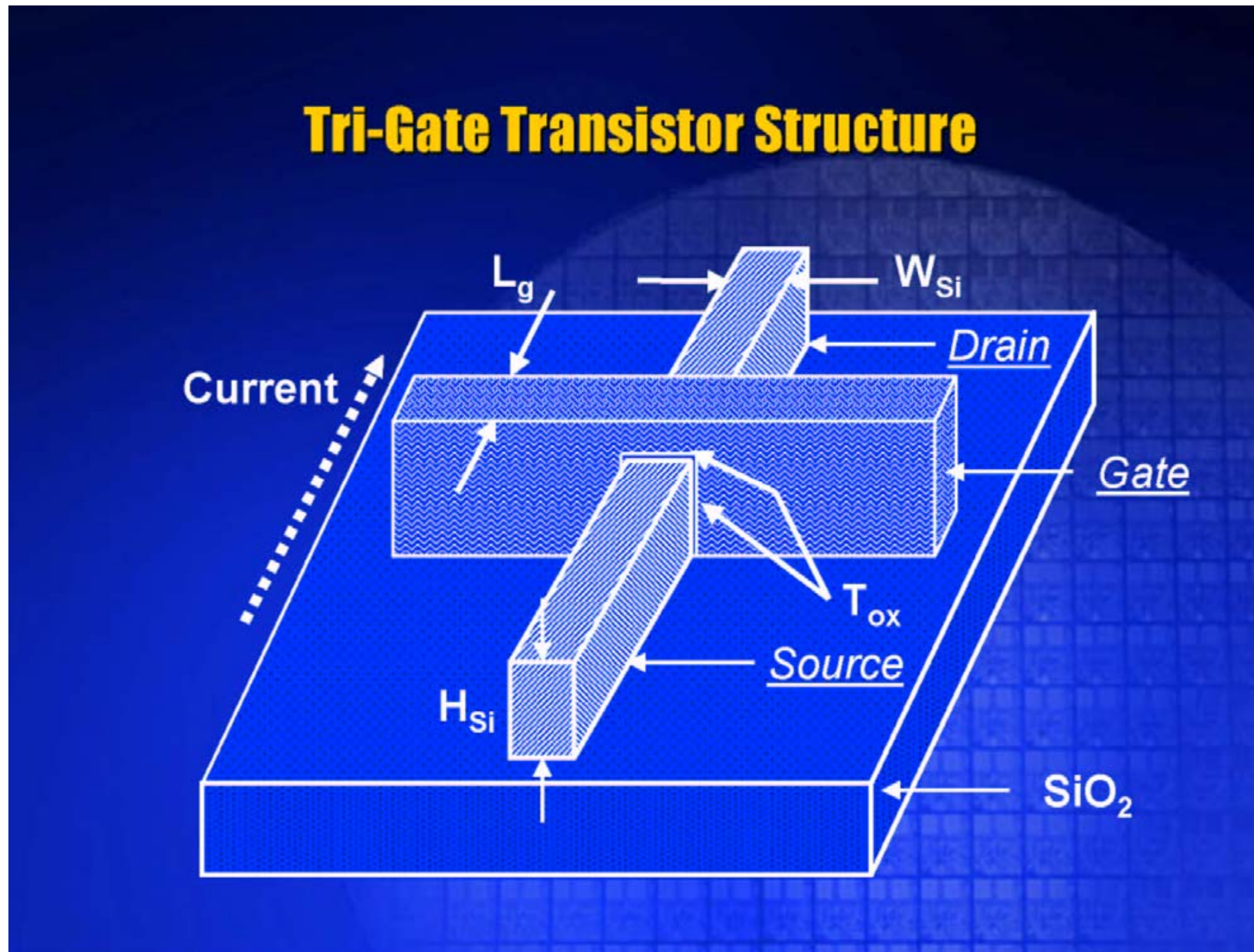
Start Dates for New Materials

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

Subject to change

"Intel's High-k/Metal Gate Announcement," November 5, 2003.



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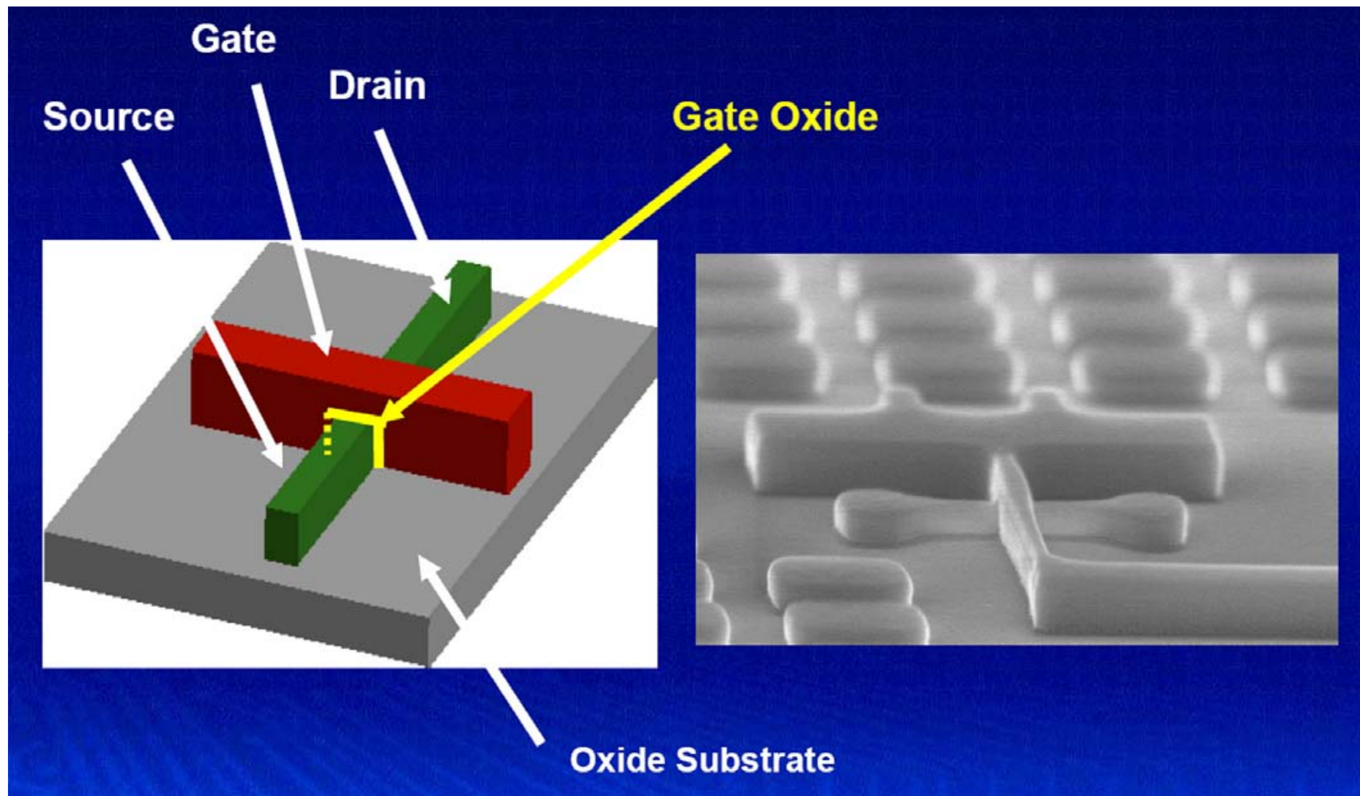
Fabricated Tri-Gate Transistor



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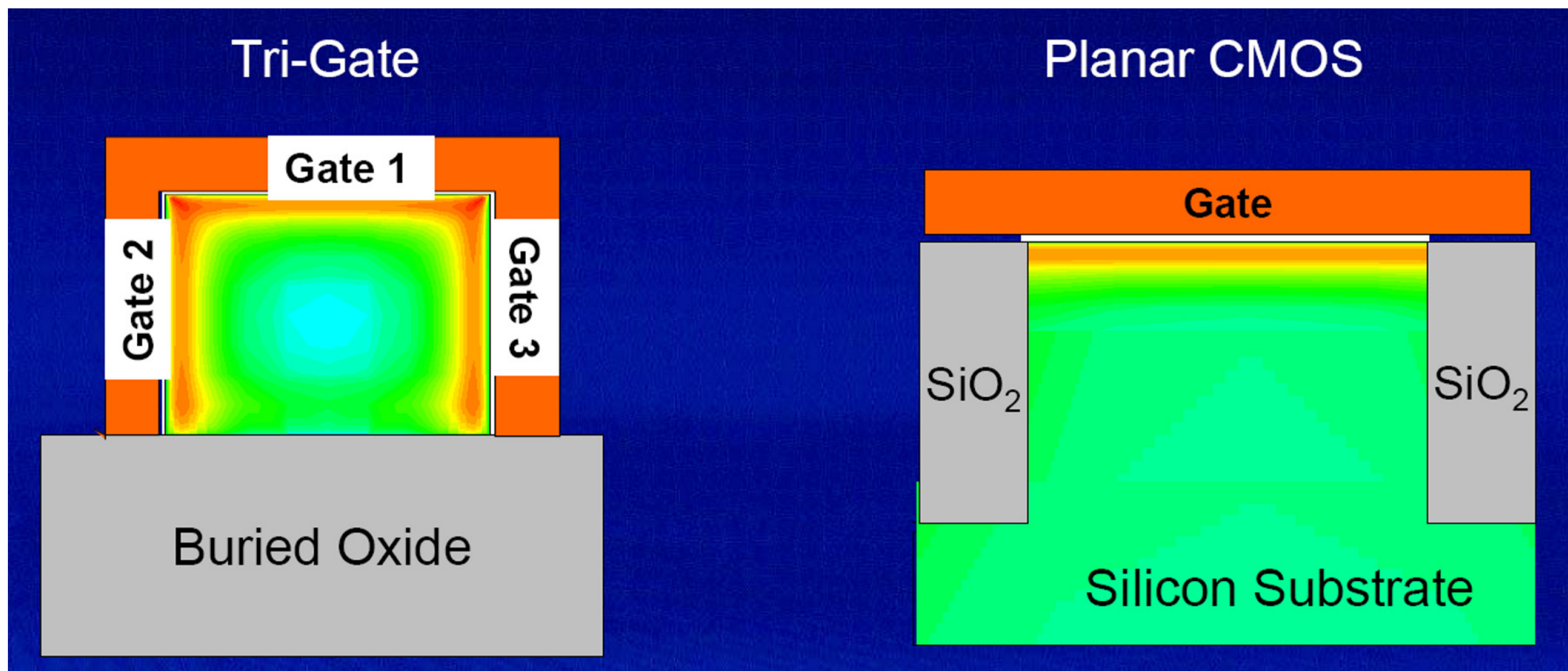
Complete Depletion of Tri-Gate Transistor



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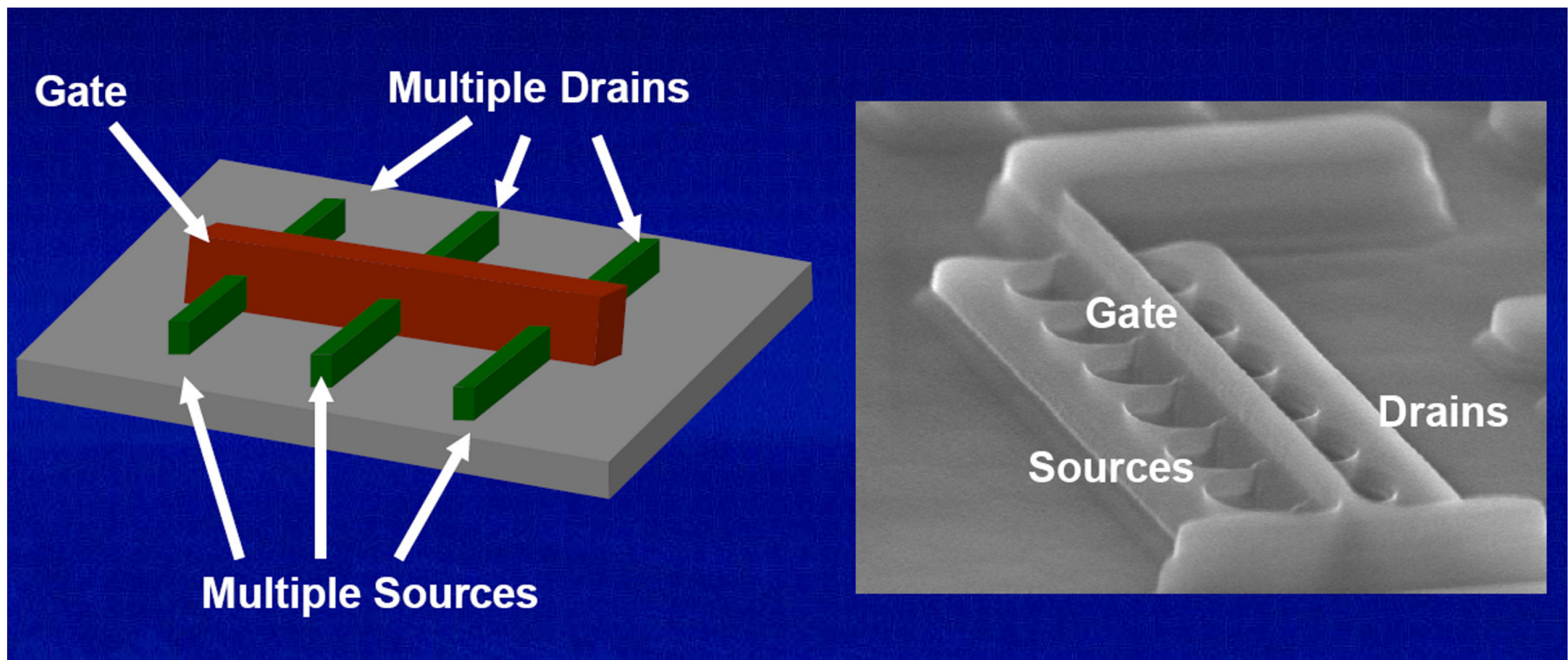
Multi-Channel Tri-Gate Transistors Enable More Drive Current



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Technology Generations to Come

Double the Density
Reduce Line Width by 0.7x

130nm→90nm→60nm→45nm→30nm→?

2 or 3 years between generations

∴

~10 ± 2 Years

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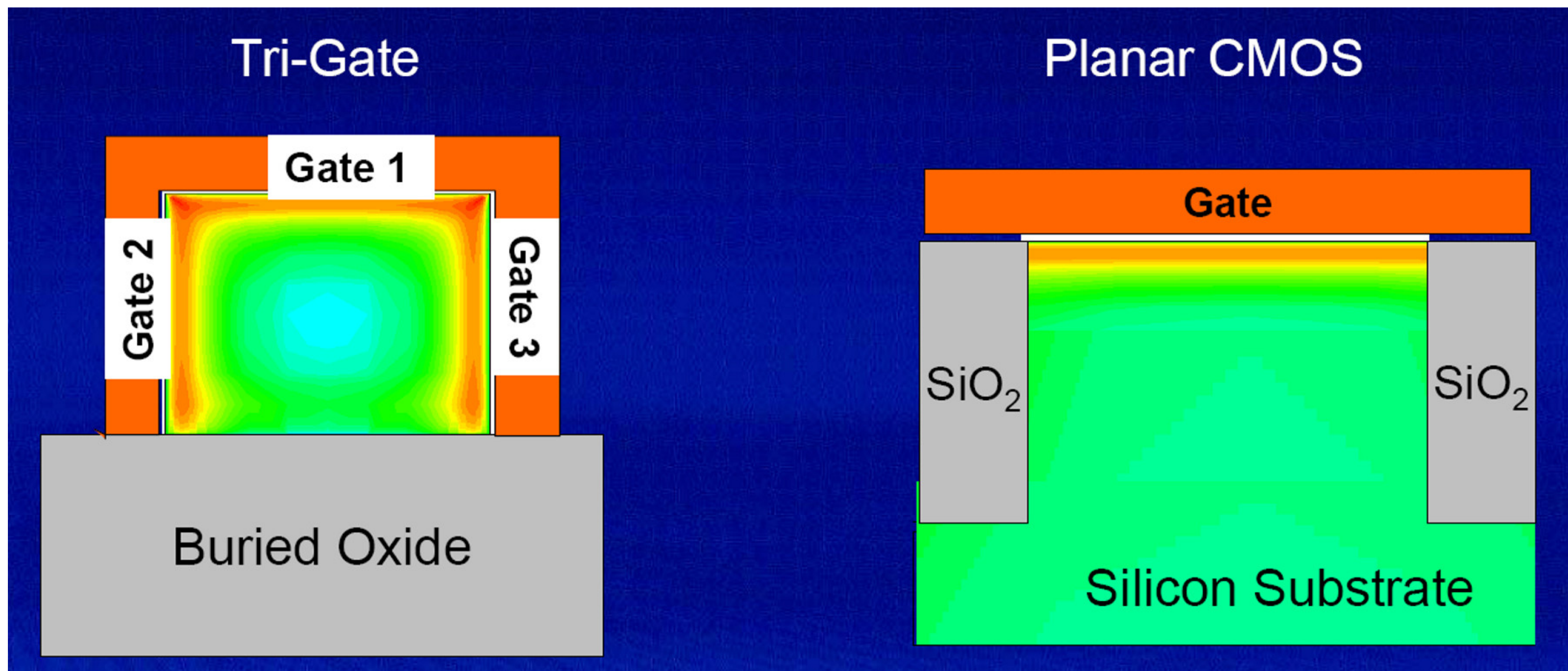

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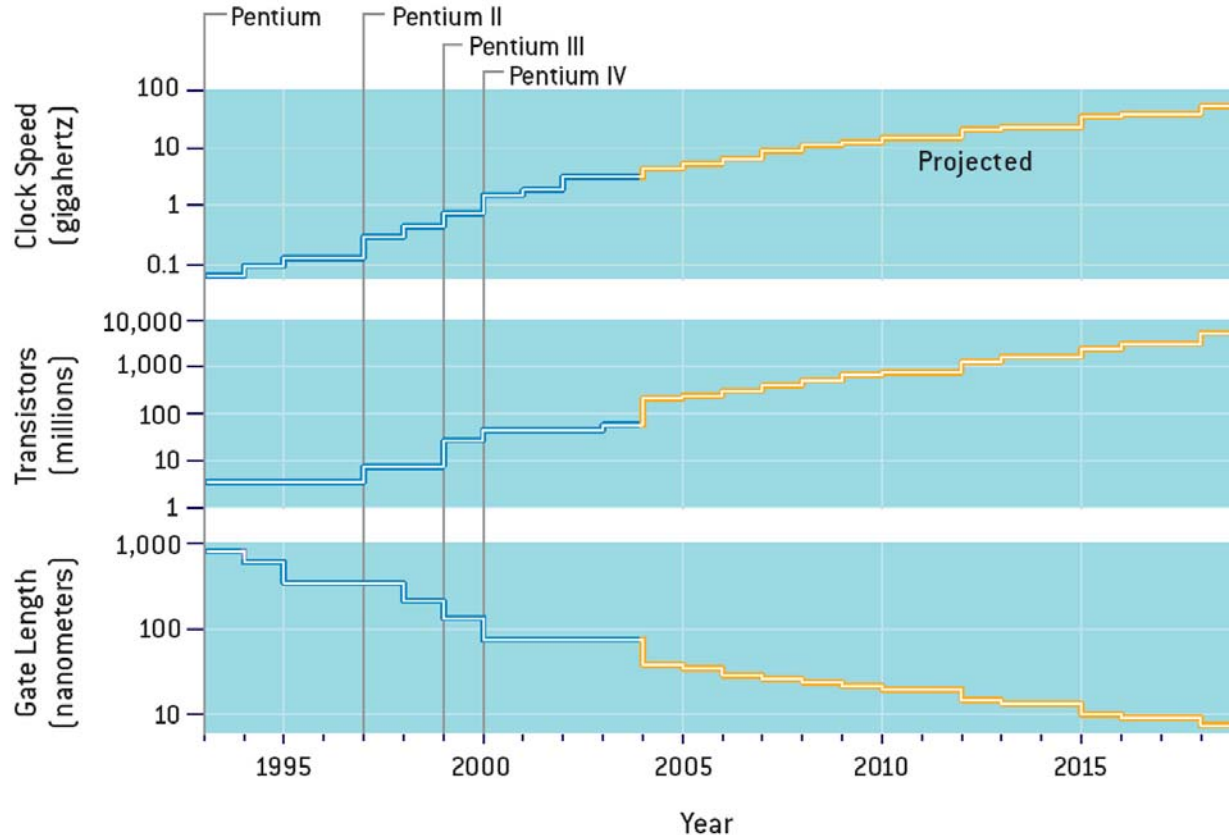
Semiconductor Industry Roadmap



G. D. Hutcheson, *Scientific American*, April, 2004, p. 76.