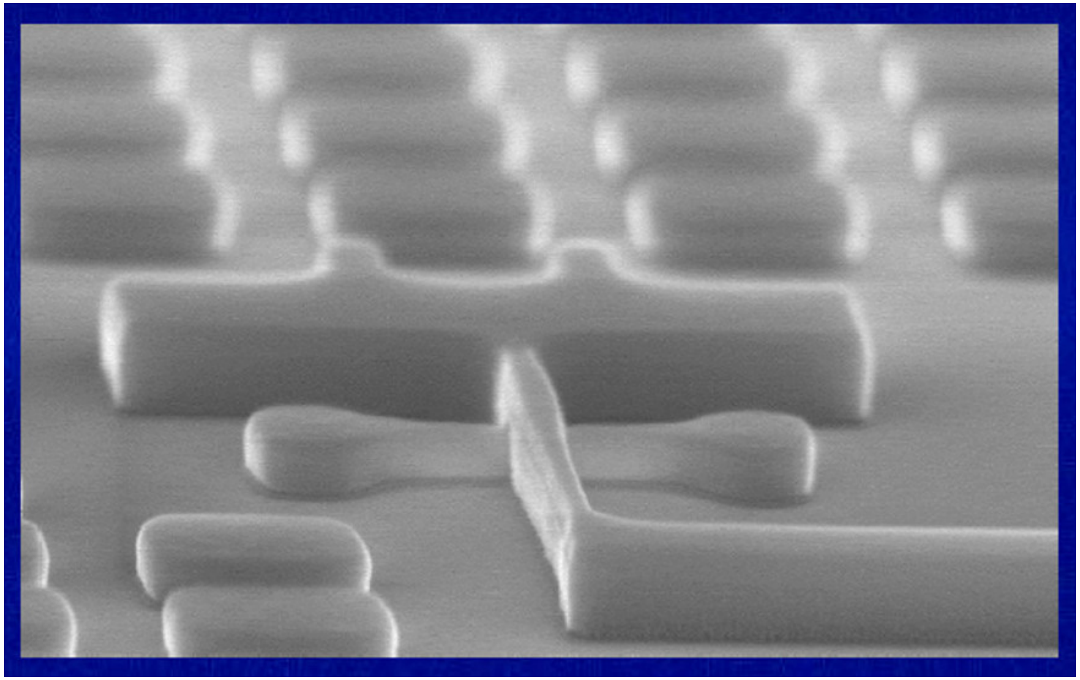
Nanomaterials

Lecture 12: Nanoscale CMOS

Nanoscale CMOS

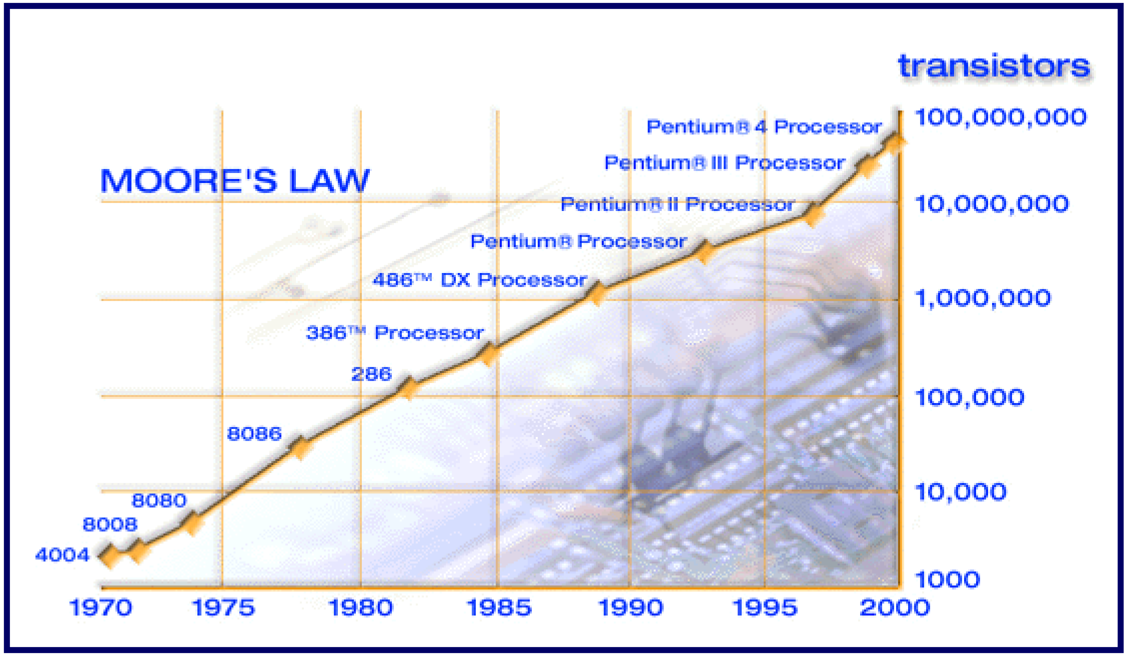


"640K ought to be enough for anybody"

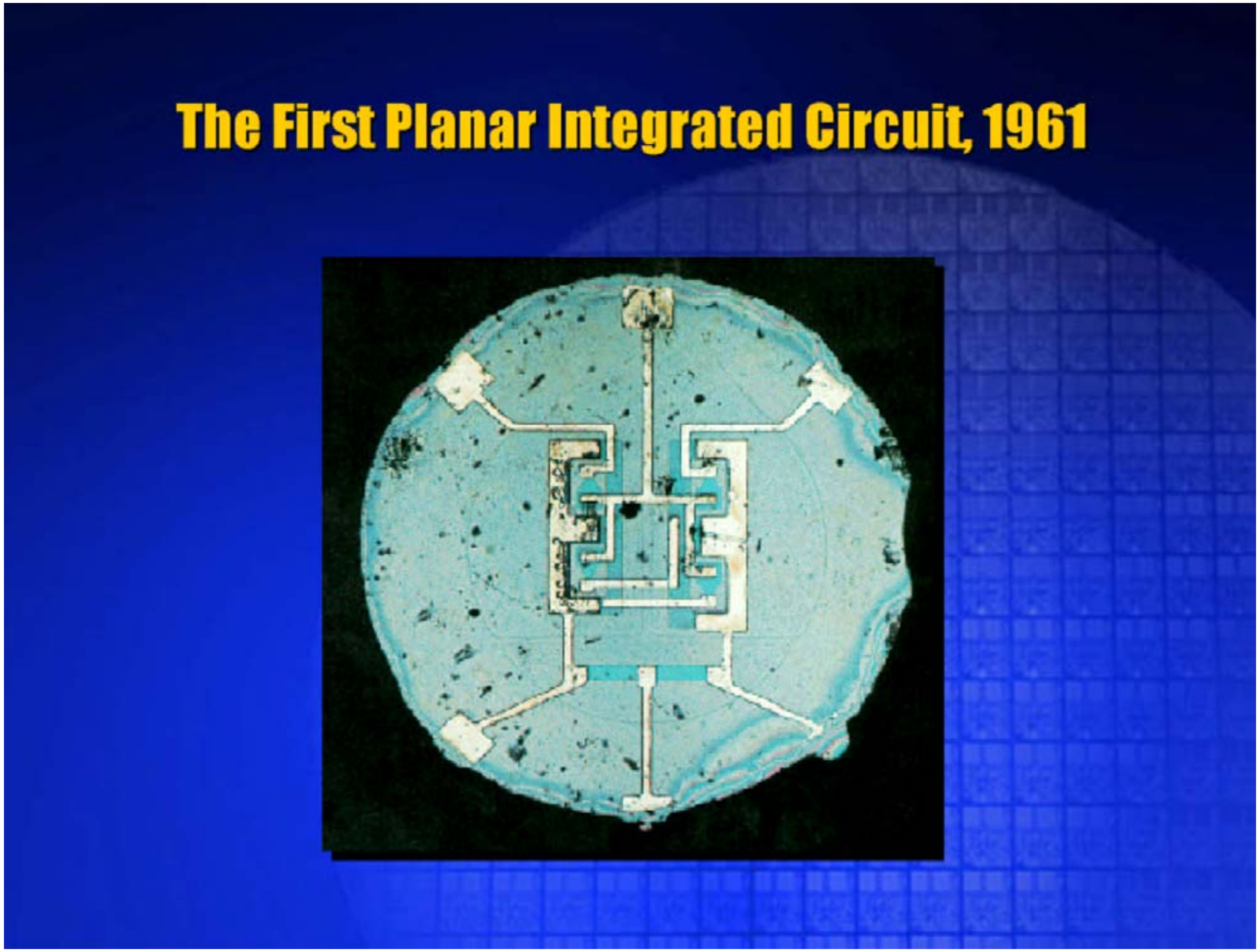
- Bill Gates, 1981

Moore's Law

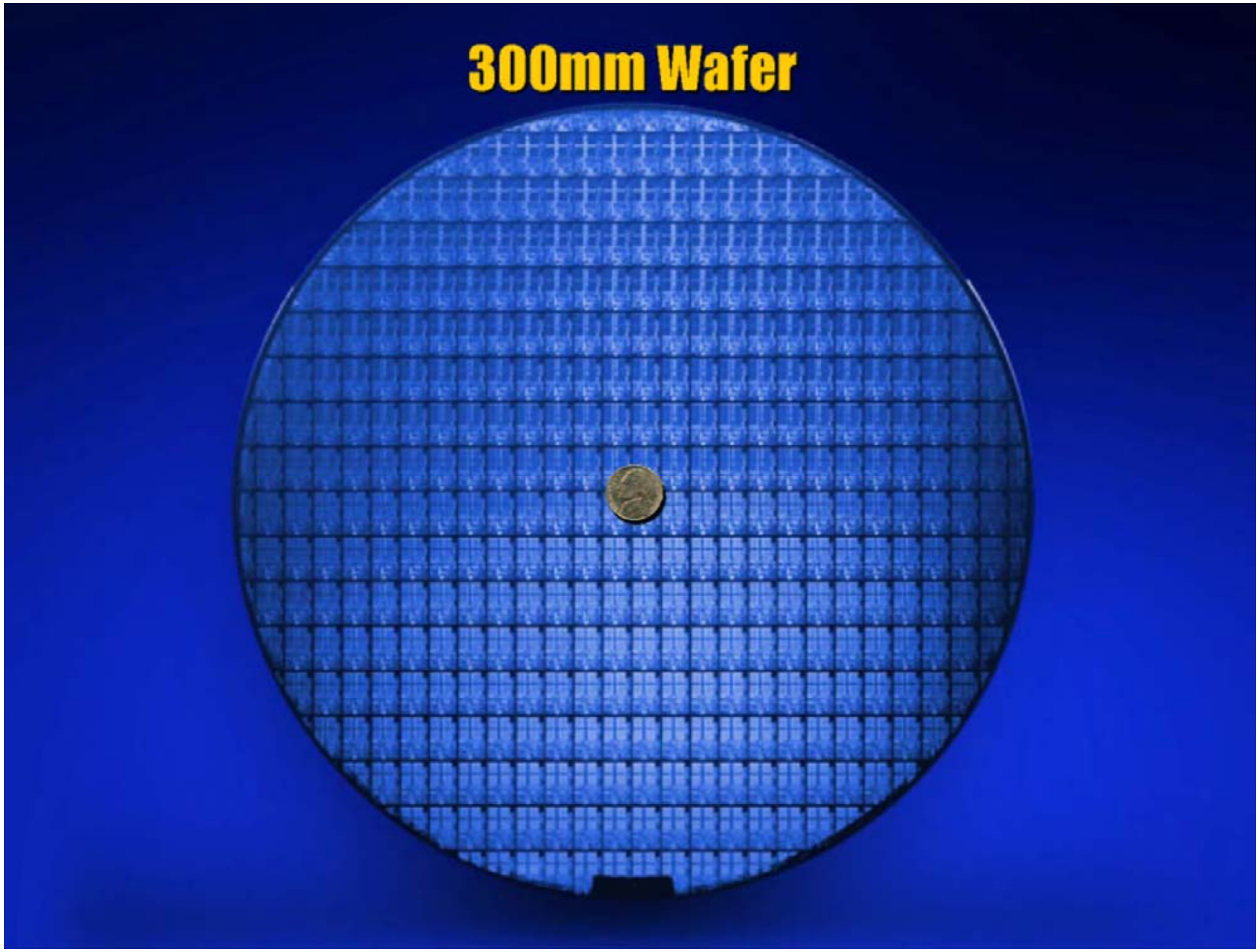
Intel Co-Founder
Gordon E. Moore



"Cramming More Components Onto Integrated Circuits"
Author: Gordon E. Moore
Publication: Electronics, April 19, 1965



“No Exponential is Forever … but We Can Delay ‘Forever’,”
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.



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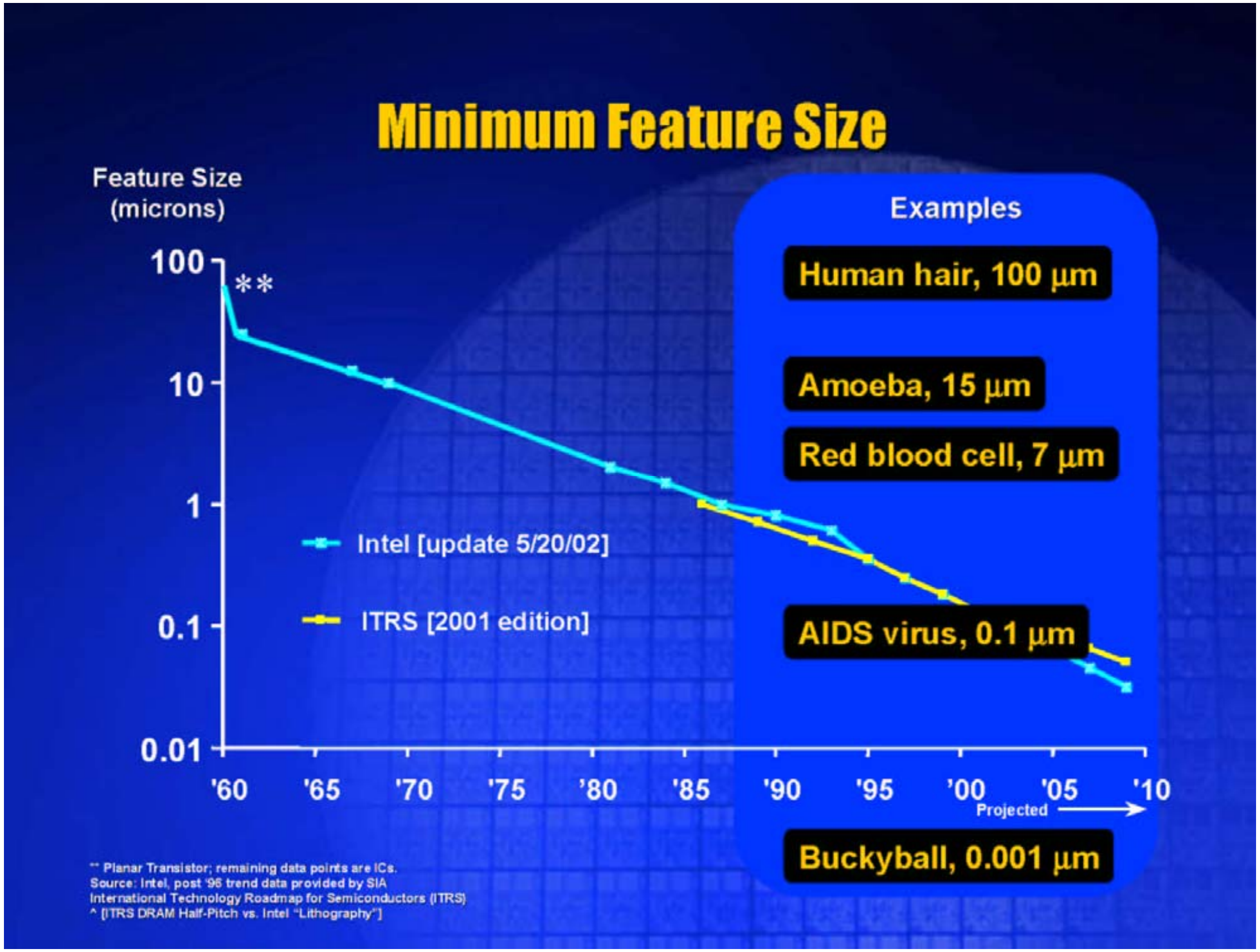

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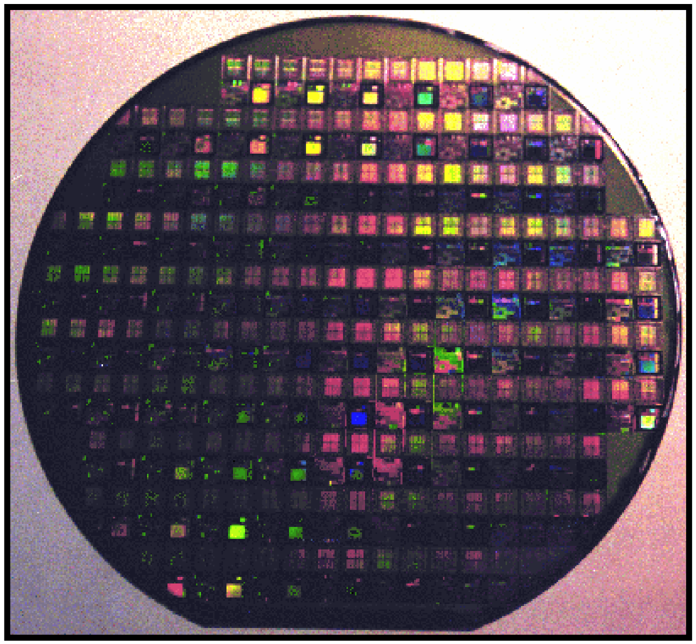
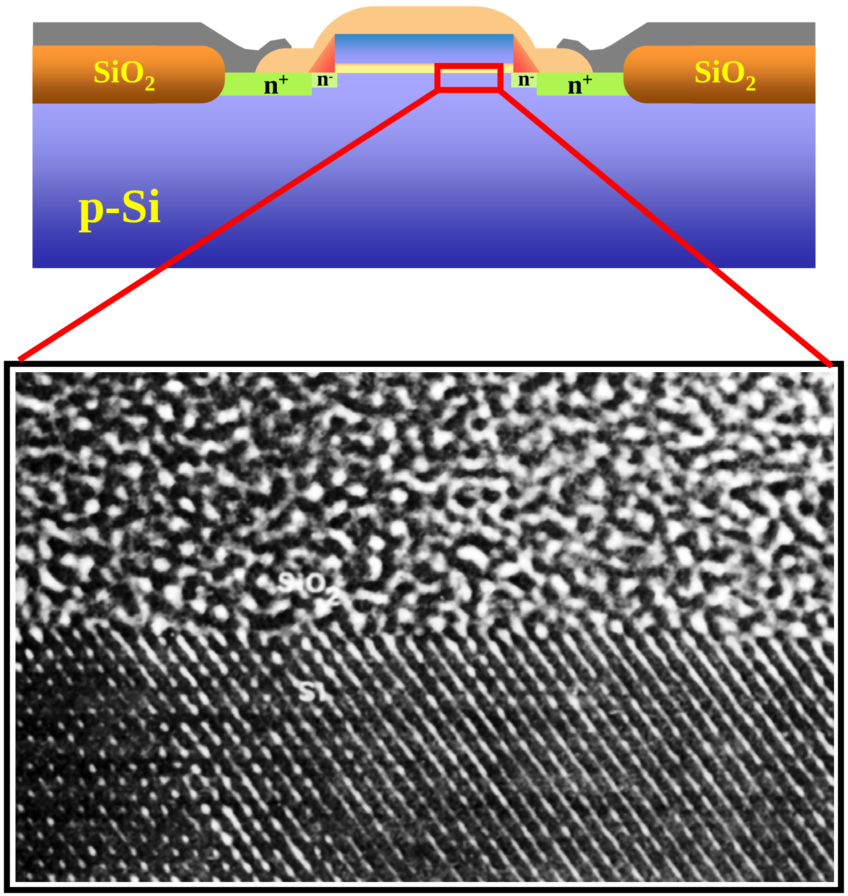
Silicon MOSFET Geometry





MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

Silicon MOSFETs

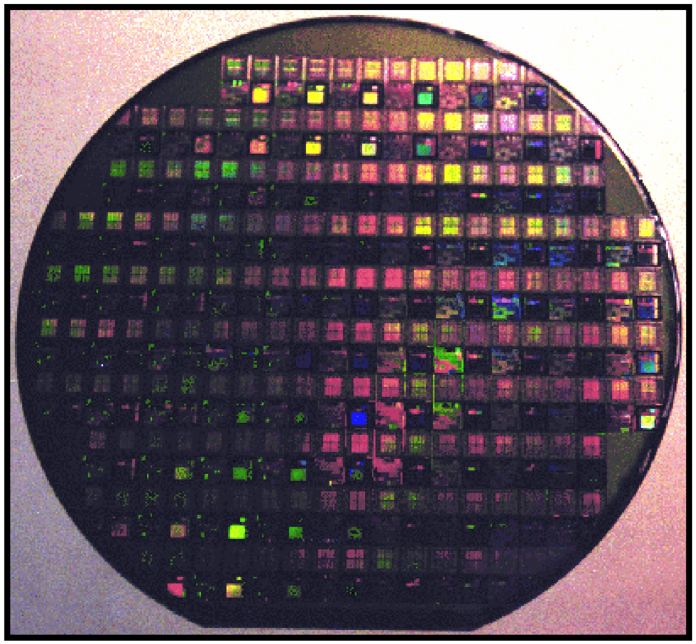
- MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

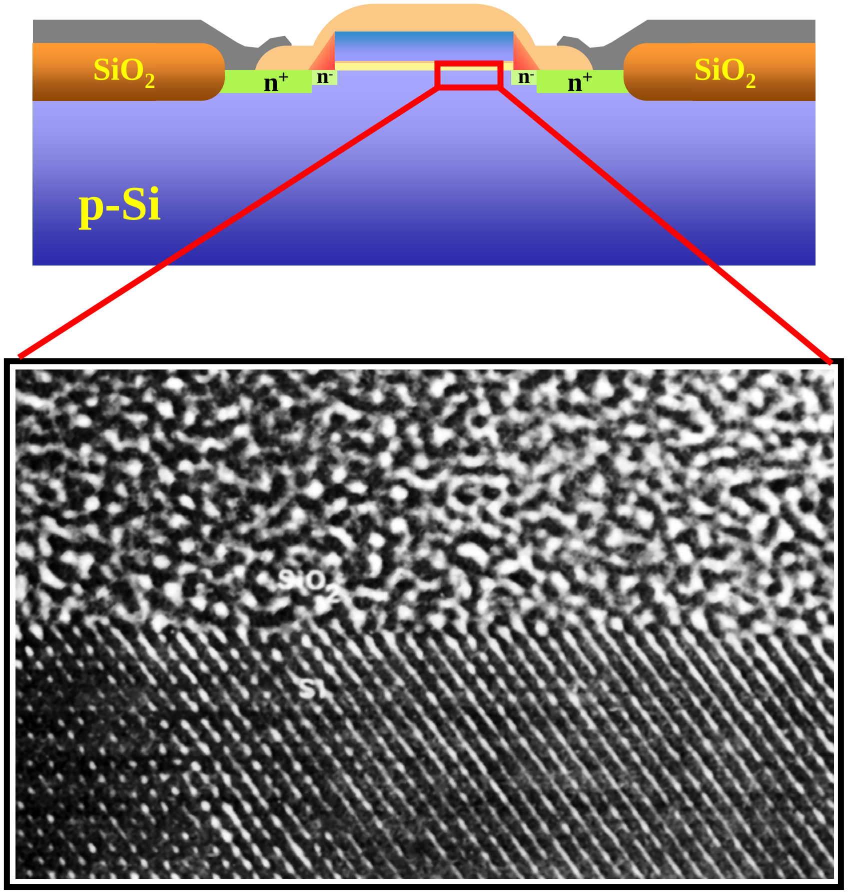
- Consider n-channel MOSFET:

  - Apply a positive voltage to gate ($V_t \sim 1$ V)
  - Negative charge is attracted to opposite side of MOS capacitor
  - The channel is inverted, creating a low resistance path from source to drain → device is “on”

NOTE: Charge is localized to the Si/SiO_2 interface
→ 2-D electron gas (2-DEG)

Silicon MOSFET Geometry





MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

Silicon MOSFETs

- All of the action occurs at the Si/SiO_2 interface
- Any spurious charge at the interface will shift the threshold voltage (i.e., turn-on voltage, V_t), disrupting the device characteristics
- For example, dangling bonds at the Si/SiO_2 interface (caused by lattice mismatch) will shift V_t
- Consequently, hydrogen is used to passivate these bonds.
- The enhanced resistance of deuterium to electron stimulated desorption is why deuterium annealing increases MOSFET lifetime

Interface States

- Although the Si/SiO_2 interface is not perfect (~10^{12} dangling bonds/cm^2), it is superior to other dielectric-semiconductor systems
- For example, Ge (Shockley proclaimed that a FET would not be practical due to high number of interface states → V_t ~ 100 V)
- Similarly, compound semiconductors suffer from the same problem
- Consequently, a different device geometry is needed for other semiconductor systems
- For example, MODFETs (modulation doped FETs)

MODFETs

- Use epitaxy to grow a compound semiconductor heterostructure (e.g., $Al_xGa_{1-x}As$ on GaAs)
- E_g (GaAs) = 1.4 eV
- E_g ($Al_{0.3}Ga_{0.7}As$) = 1.8 eV
- $\Delta E_c \sim 0.24$ eV (given by difference in electron affinity)
- Discontinuity in conduction band creates a triangular quantum well → confinement of electrons → 2-DEG

MODFET Schematic and Band Profile

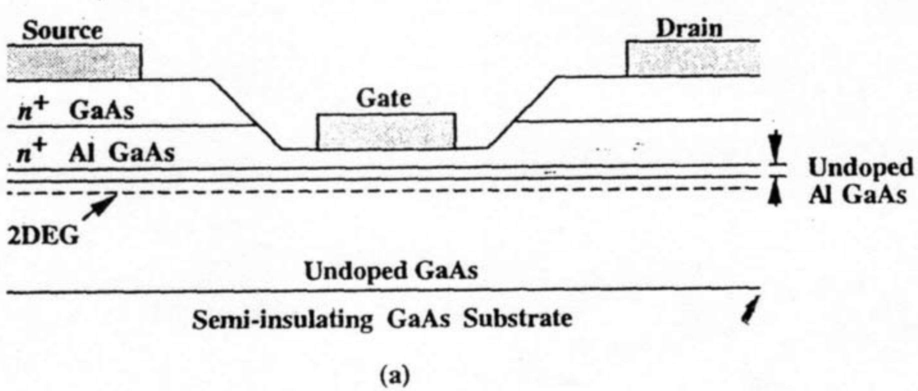


Figure 1: A schematic of a GaAs/AlGaAs MODFET.

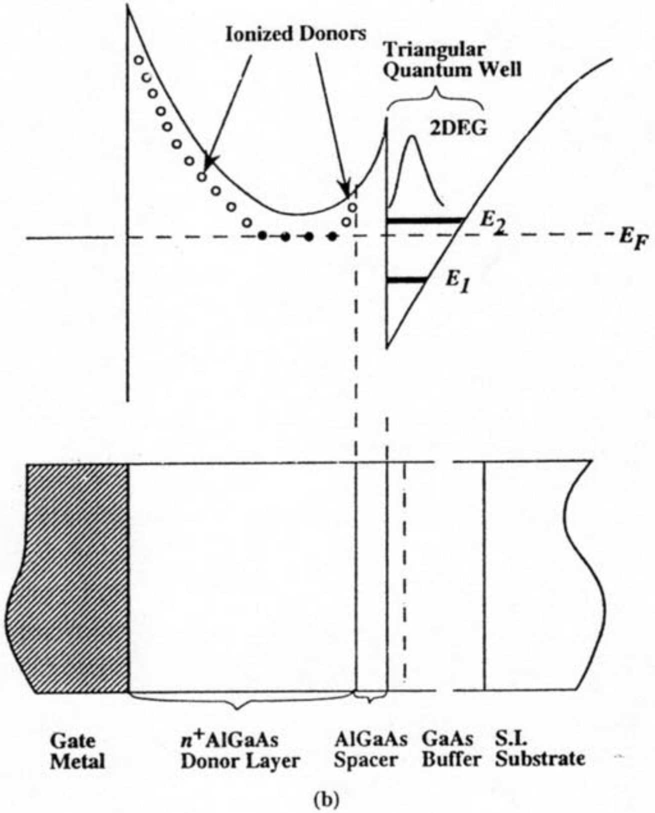


Figure 2: The band profile of a MODFET showing bandbending leading to a triangular quantum well at the GaAs/AlGaAs interface.

MODFET Advantages and Disadvantages

Advantages:

(1) 2-DEG → High electron density
(2) Free carriers are spatially separated from dopants
→ Minimal ionized impurity scattering
(3) High speed devices (e.g., used in communication systems)
(4) Direct bandgap → optoelectronic applications

Disadvantages:

(1) The equivalent p-channel device is not easily integrated, unlike silicon where p-channel is realized via doping
(2) MODFET-based logic requires more power than silicon

Complementary MOS (CMOS)

* Silicon is the most widely material for microprocessors and other logic circuitry because it can implement CMOS architectures

Simplest logic gate:
INVERTER

$$V_{in} = V_{DD} \rightarrow V_{out} = 0\ \text{V}$$

$$V_{in} = 0\ \text{V} \rightarrow V_{out} = V_{DD}$$

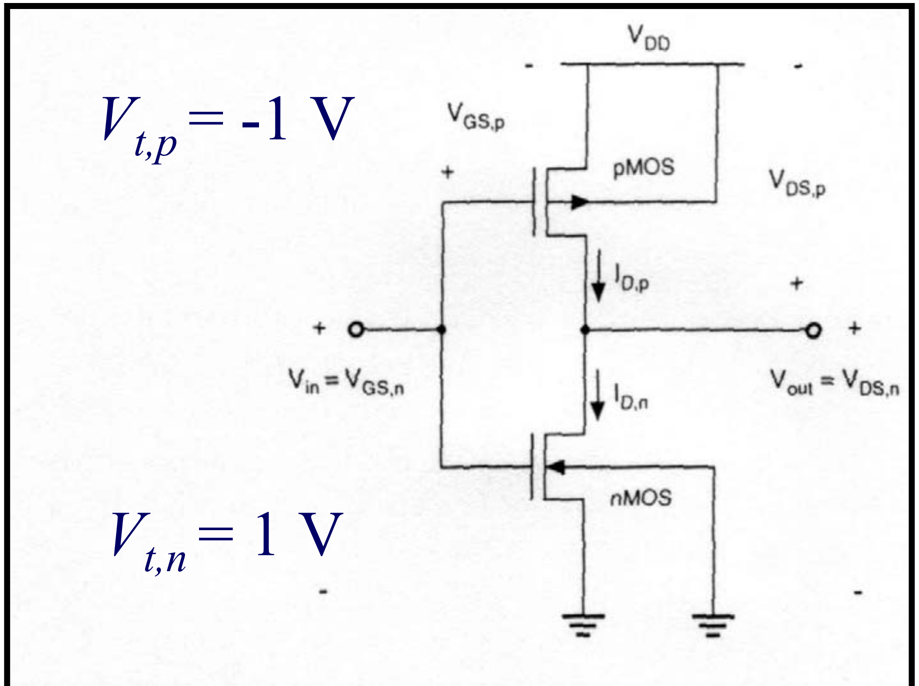


Figure 5.19. CMOS inverter circuit.

S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill Company (1996).

Why CMOS?

- In steady-state, there is no path from VDD to ground
- Consequently, power is only dissipated during switching (Note: power dissipation increases with speed)
- Without CMOS, power is dissipated when input is high:

$$V_{in} = V_{DD} \rightarrow P = V_{DD}^2/R$$

Highly integrated logic circuits require CMOS

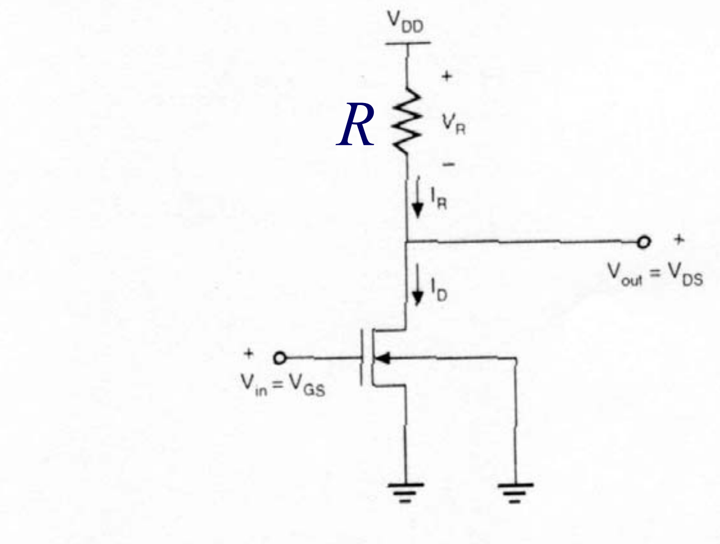


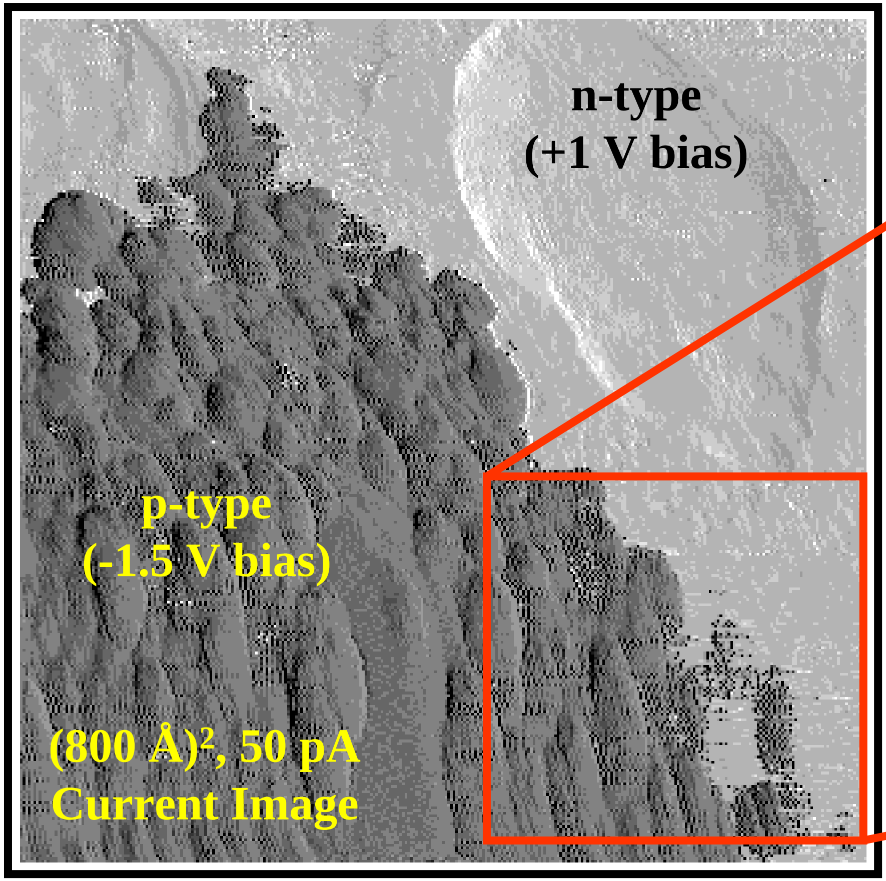
Figure 5.7. Resistive-load inverter circuit.

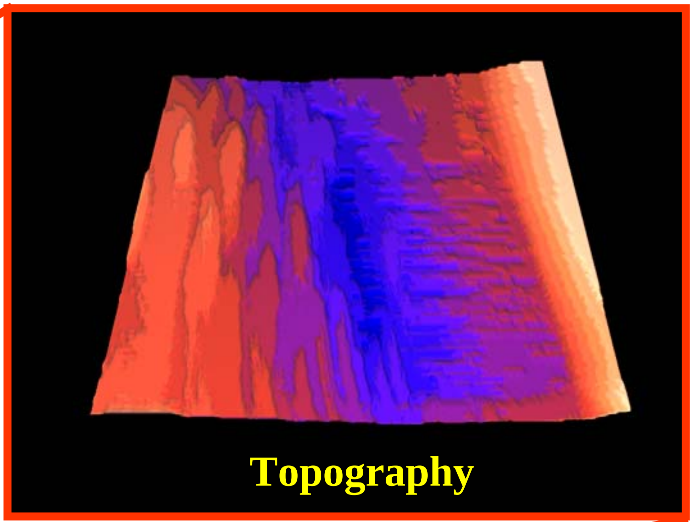
S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill Company (1996).

Limitations of CMOS at the Nanoscale

(1) Statistical variations in dopants:

Substrate: Si(100), p-type, B-doped (~ 0.01 Ω-cm)
Processing: 1.) Phos. predep @ 1000°C for 10 min.
2.) Phos. drive @ 1000°C for 10 min.
3.) ~ 1000°C anneal in UHV for 1 min.





Limitations of CMOS at the Nanoscale

(2) Gate oxide scales with channel length

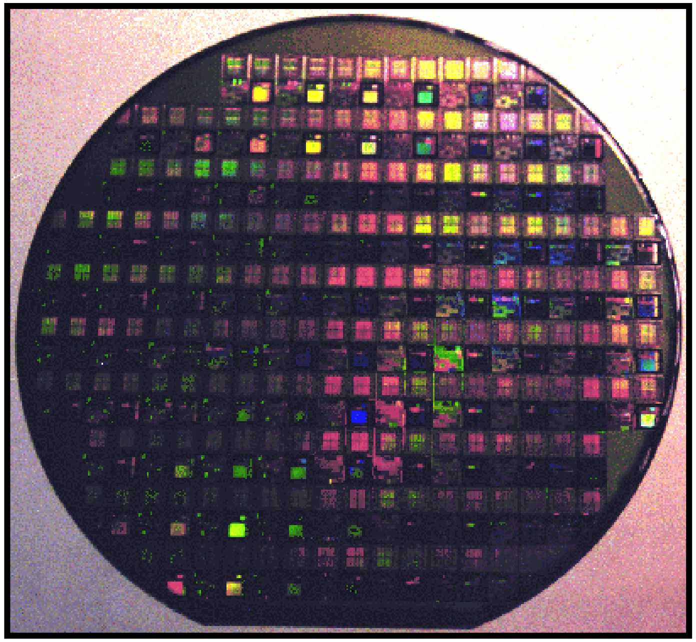
(At ~ 1 nm gate oxide thickness, large gate leakage current due to tunneling)

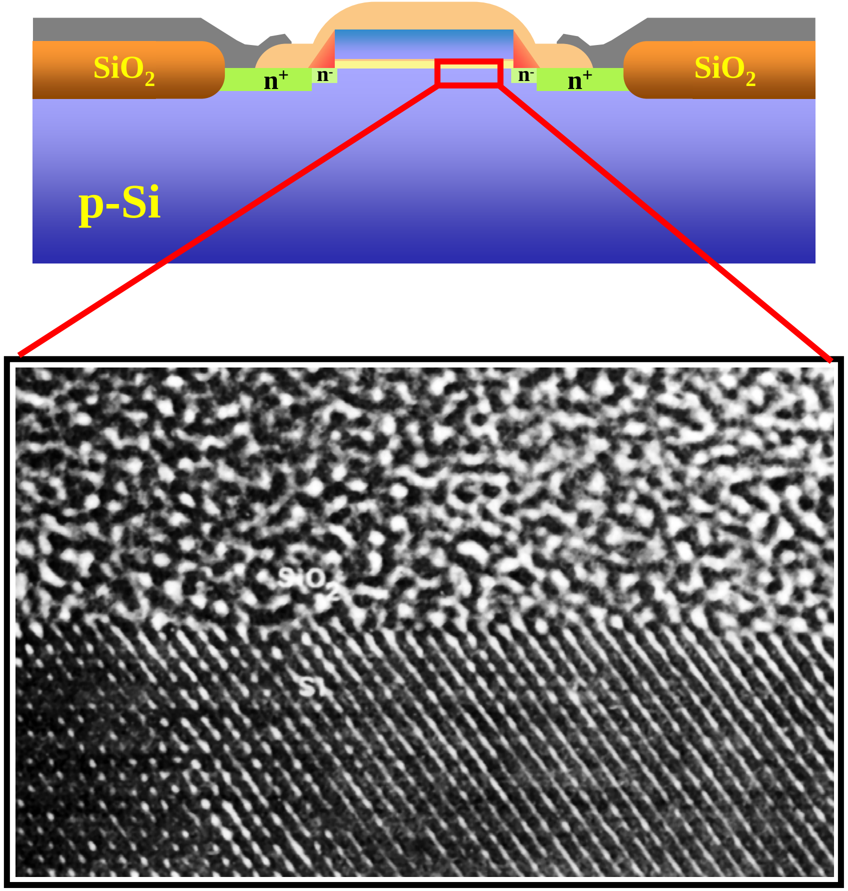
NOTE: $C_{ox} = \varepsilon_{ox} A / d_{ox}$

(Rather than decrease d_{ox}, increase ε_{ox})

→ High-k dielectric materials

Silicon MOSFET Geometry





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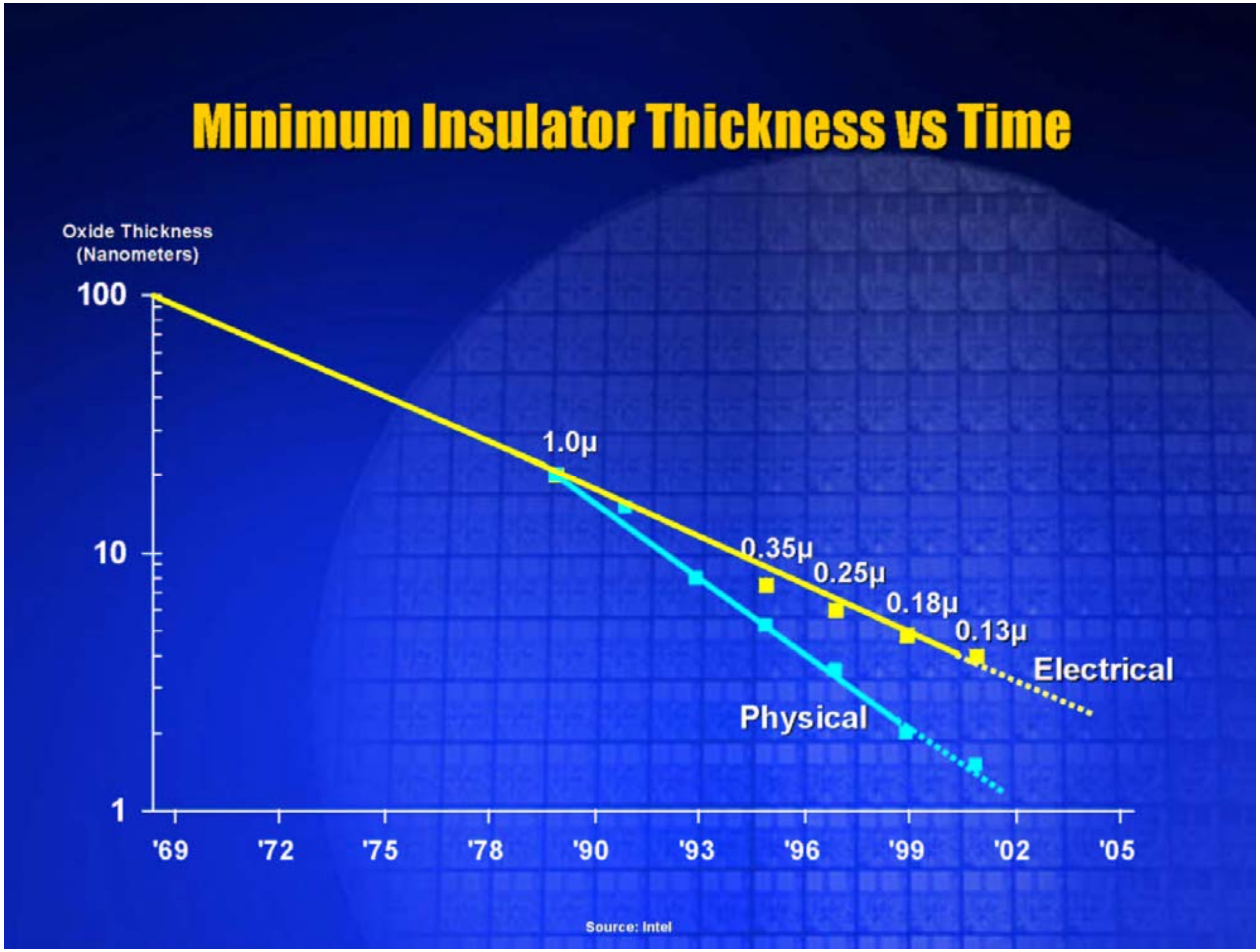

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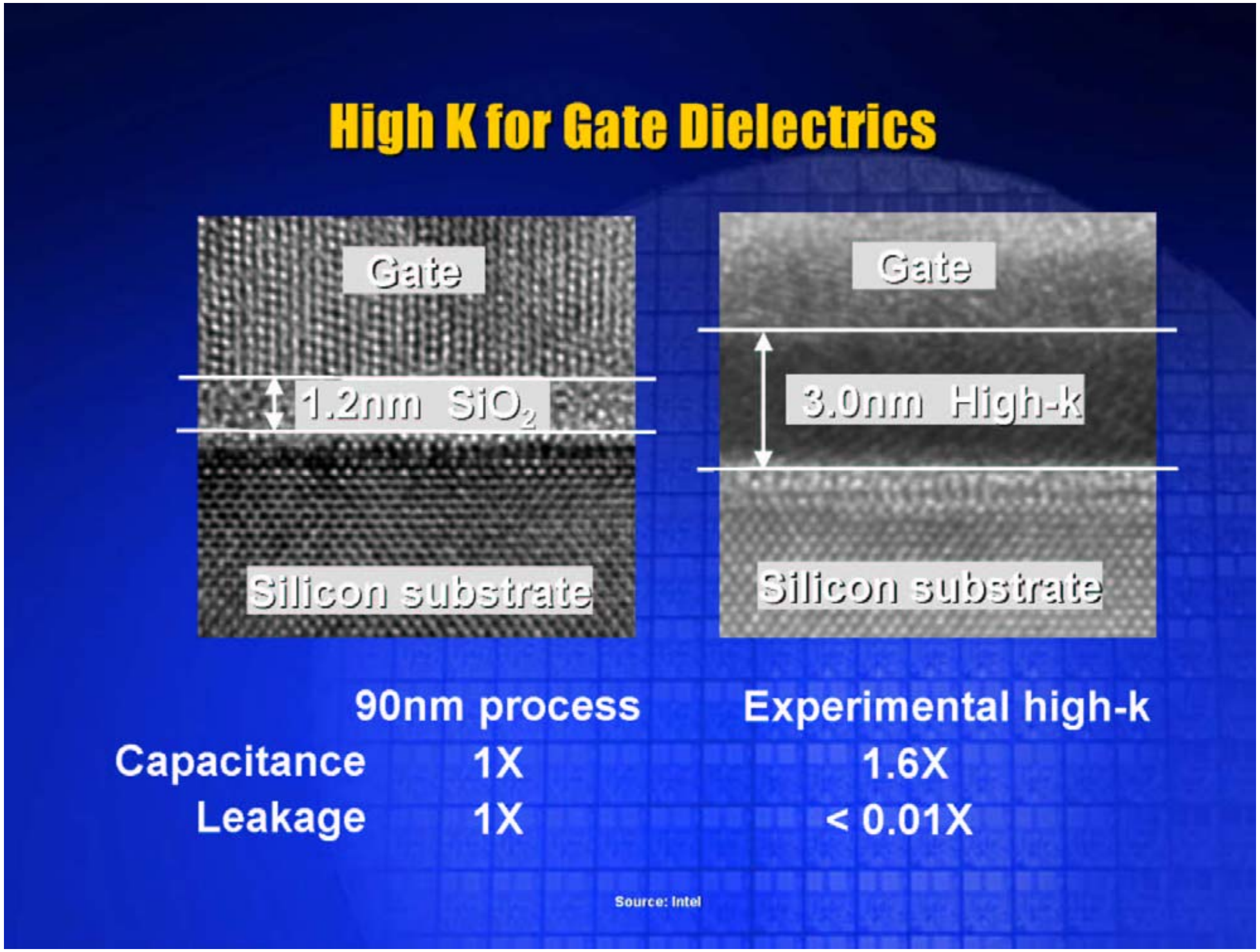

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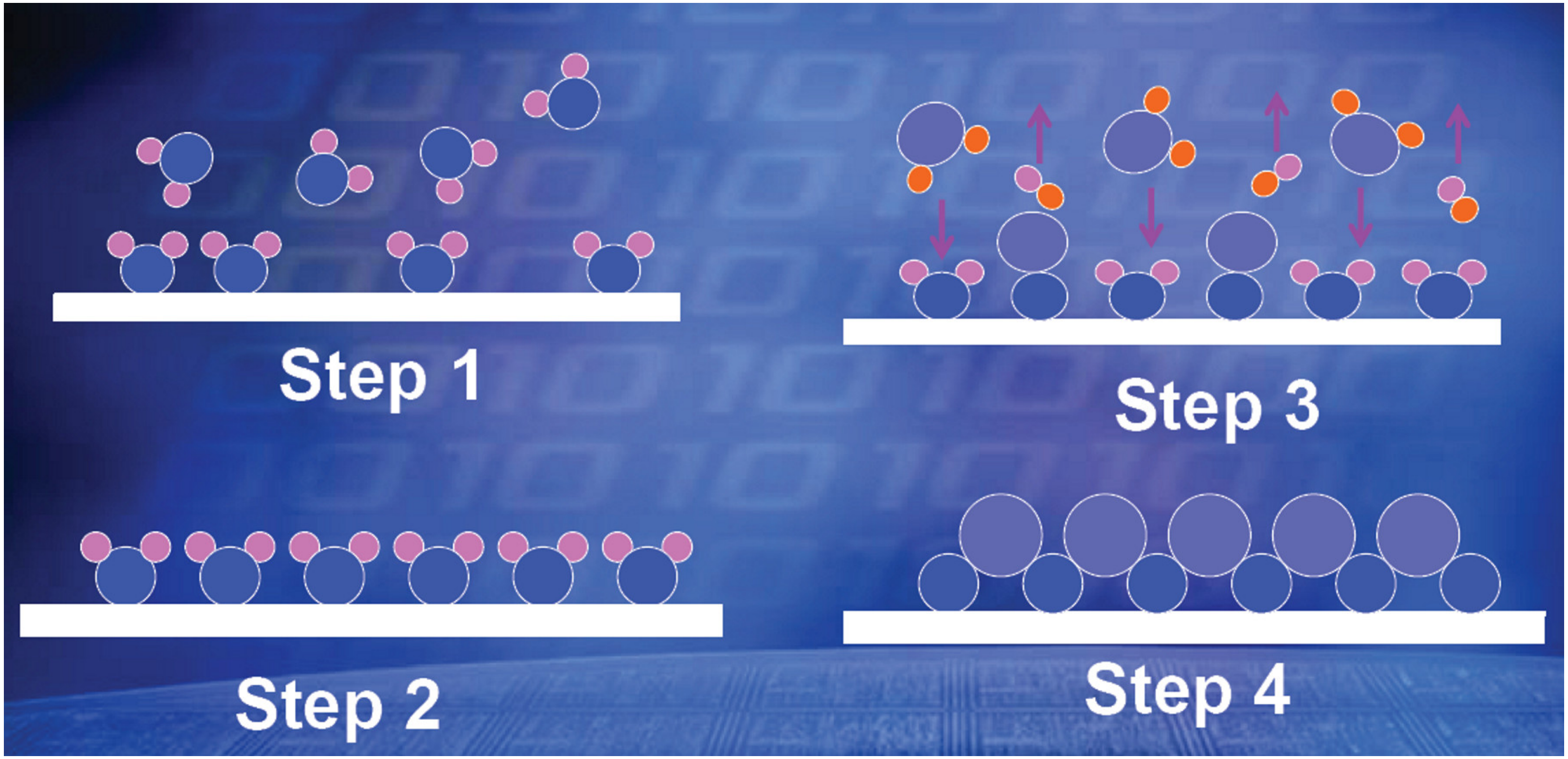
Atomic Layer Deposition of High K Dielectrics



"Intel's High-k/Metal Gate Announcement," November 5, 2003.

Problems with High K Dielectrics

Two new interfaces:

(1) Interface between high k dielectric and silicon needs to be as free of dangling bonds as possible

(2) Interface between high k dielectric and poly silicon gate leads to two problems:

(a) Phonon scattering, which decreases speed

(b) Threshold voltage is pinned to high values

Integrating High K Dielectrics with Metal Gate Electrodes

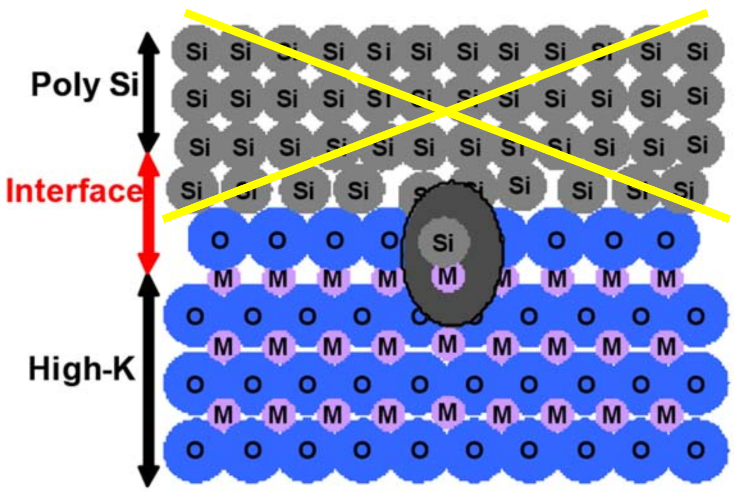


Fig. 4 Defect formation at the polySi and high-K dielectric interface is most likely the cause of the Fermi level pinning which causes high threshold voltages in MOSFET (M = Zr or Hf).

Replace poly Si with a metal gate whose work function minimizes Fermi level pinning

Different metals are required for NMOS and PMOS

R. Chan, "Advanced metal gate/high-k dielectric stacks for high-performance CMOS transistors," AVS 5th International Conference on Microelectronics and Interfaces, Santa Clara, California, March 1, 2004.

Limitations of CMOS at the Nanoscale

(3) Interconnects scale with channel length

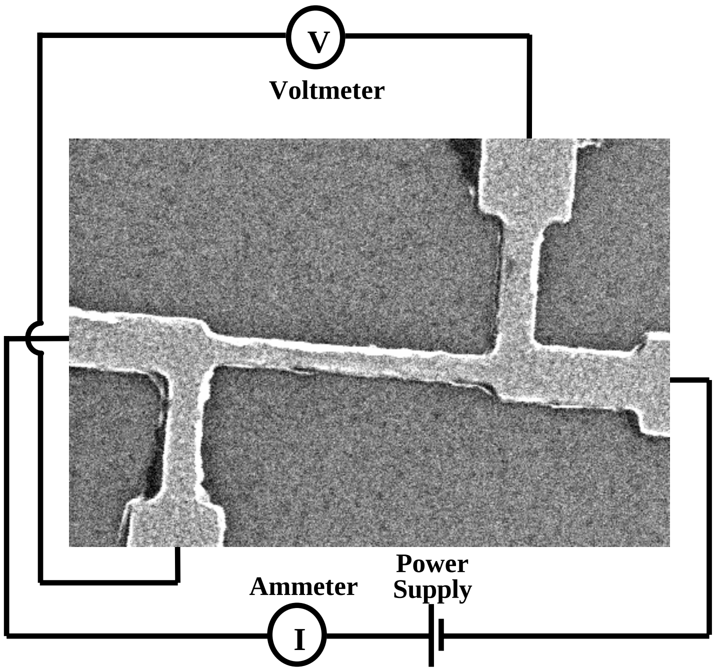
→ Higher $J = I/A$, $R = \rho l/A$

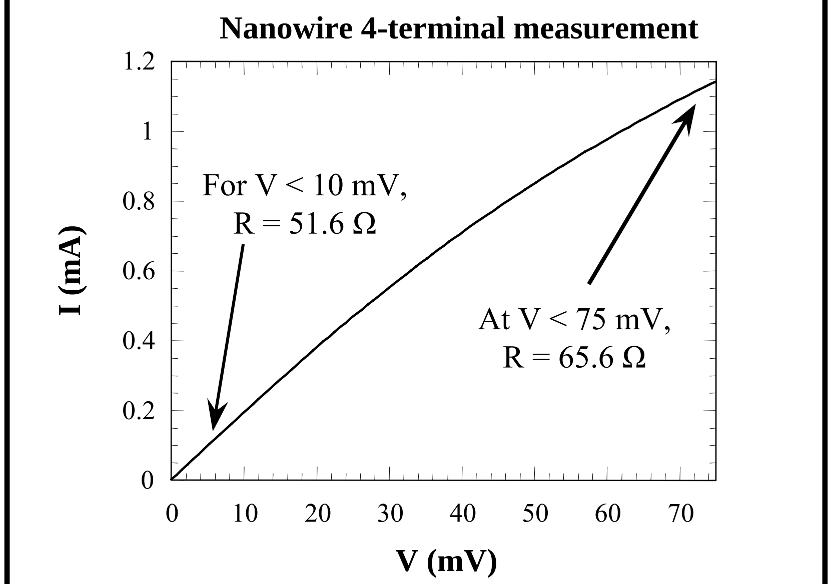
→ electromigration and other failure mechanisms

→ electromigration concerns motivated the switch from aluminum to copper interconnects

Electrical Characterization of Gold Nanowires

Biasing circuit diagram:



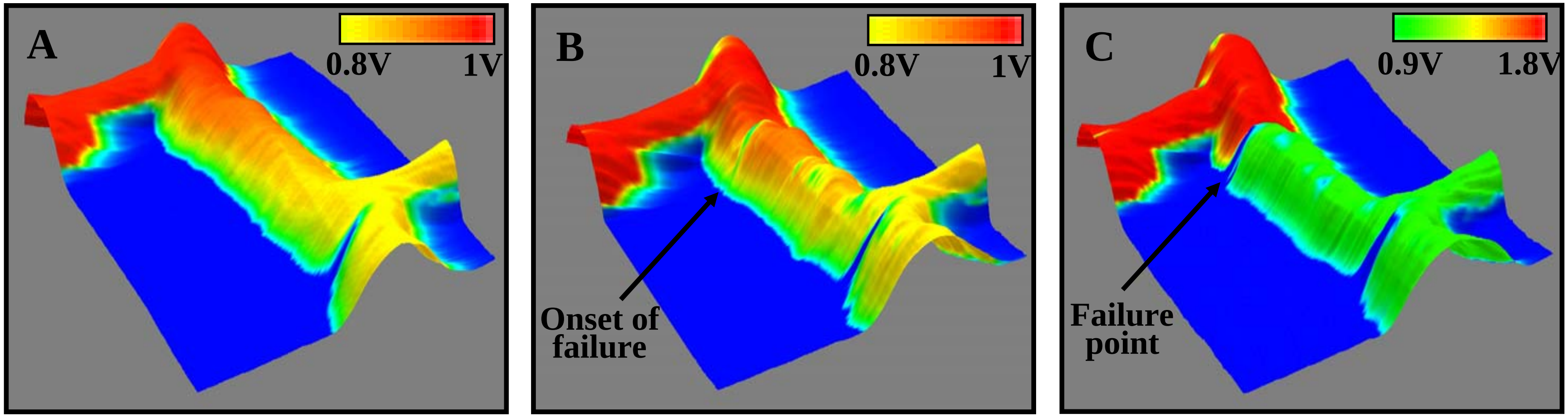


Nanowire parameters:
length = 1 μm, width = 60 nm, thickness = 20 nm

- Nanowire resistivity = 6.2 μΩ-cm > bulk gold resistivity = 2.2 μΩ-cm
- Grain boundary scattering is the dominant contributor to the observed resistivity enhancement.
- Nanowire resistance increases at high bias near failure.

Potentiometry of Nanowire Failure

Evolution of nanowire failure:

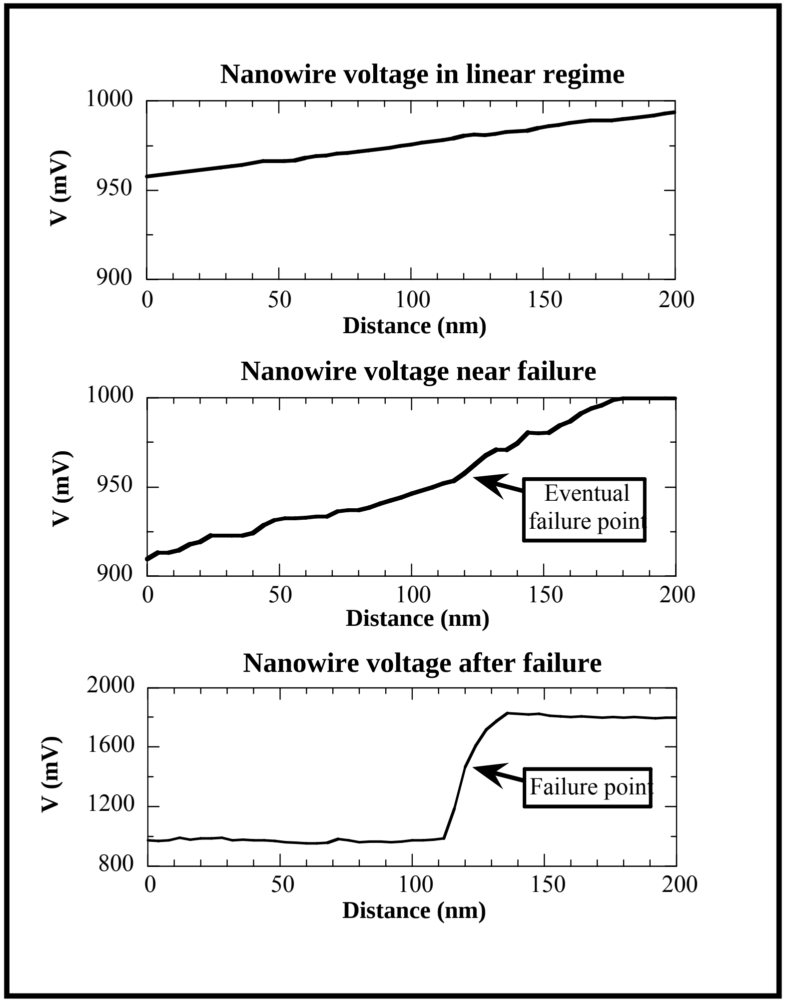


Contact mode AFM potentiometry images: Wire width = 60 nm

(Breakdown current density = 3.75×10^{12} A/m^2).

M. C. Hersam, A. C. F. Hoole, S. J. O'Shea, and M. E. Welland, *Appl. Phys. Lett.*, 72, 915 (1998).

Mechanism of Nanowire Failure



Characteristics of line plots of potential across the failure point:

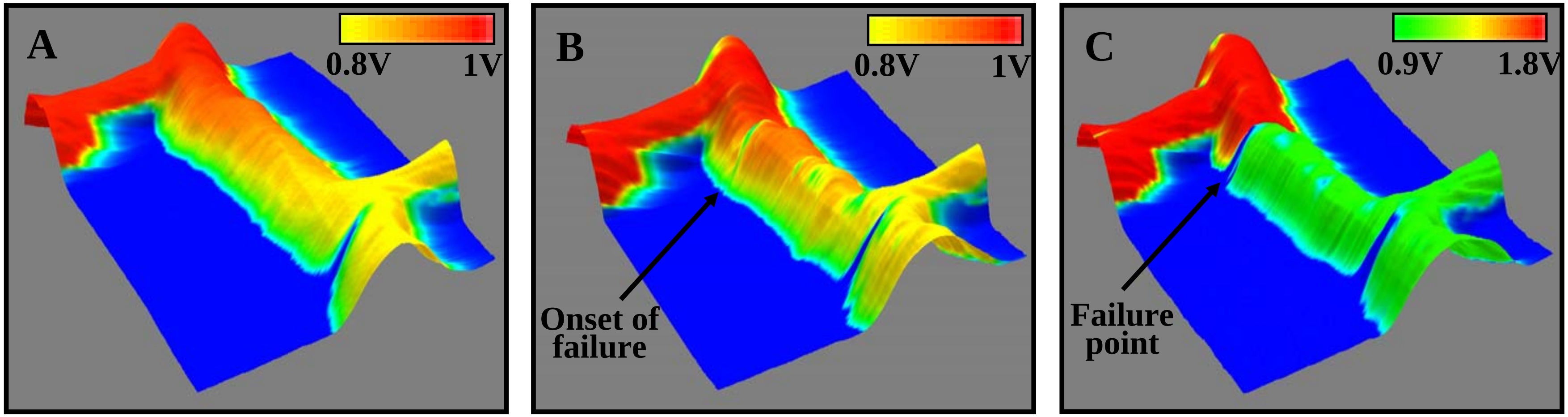
- Essentially linear behavior at low bias.
- Near failure, a discontinuity in the potential gradient is detected.

Proposed Failure Mechanism:

- Localized power dissipation in the failure region creates a temperature gradient that enhances electromigration.
- This is a self-perpetuating process that rapidly leads to failure.

Potentiometry of Nanowire Failure

Evolution of nanowire failure:



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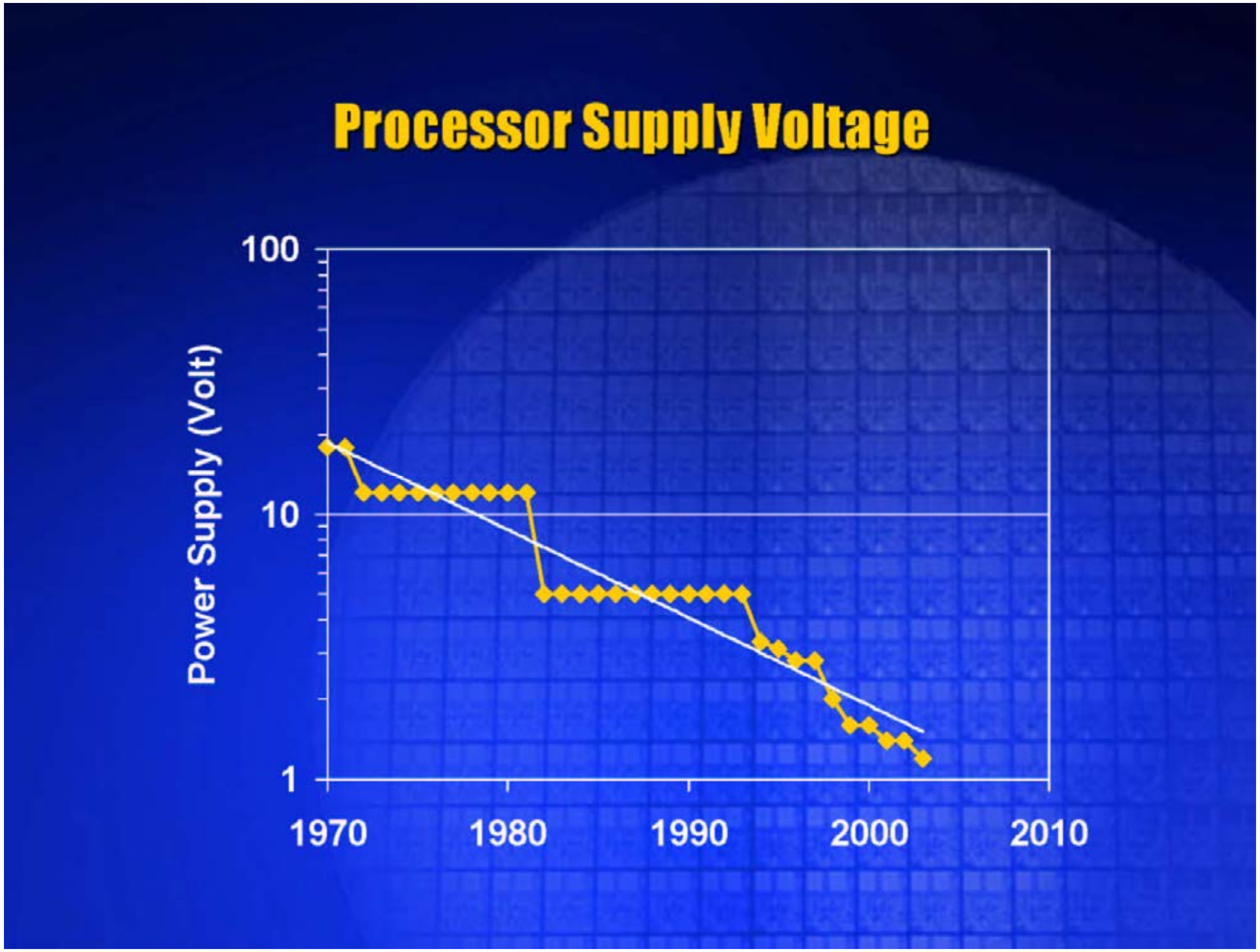
Limitations of CMOS at the Nanoscale

(4) Hot electron effects

→ As channel length decreases, E-field increases ($E = V/l$)

→ "Hot electrons" desorb hydrogen at interface (replace with deuterium to increase lifetime)

→ Alternatively, decrease V → implies tighter control of noise and device characteristics



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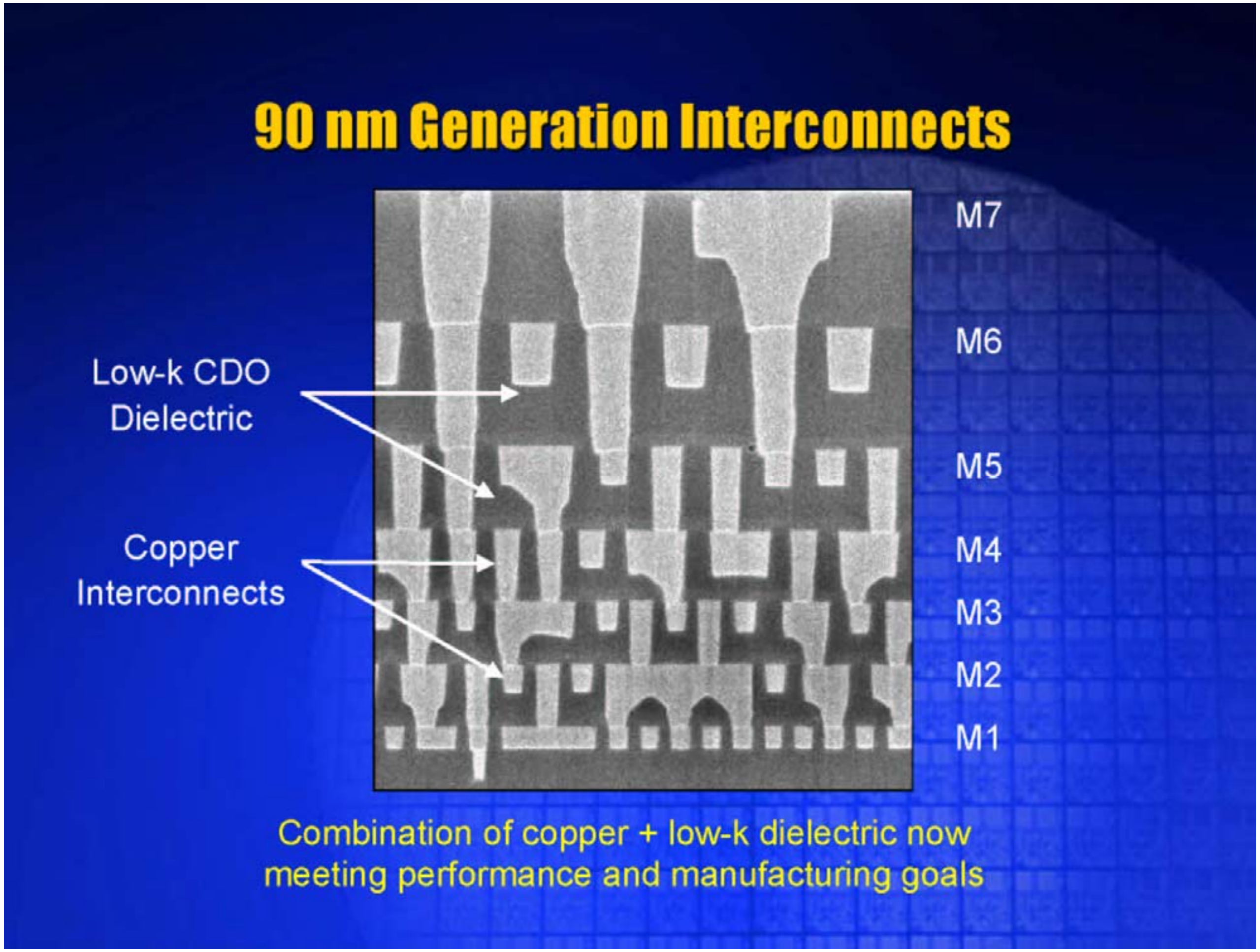
Limitations of CMOS at the Nanoscale

(5) Interconnect cross-talk

→ Capacitive coupling increases as spacing between interconnects decreases ($C = \varepsilon A/d$)

→ To decrease d, ε needs to be decreased

→ Low-k dielectric materials (porous materials)



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Limitations of CMOS at the Nanoscale

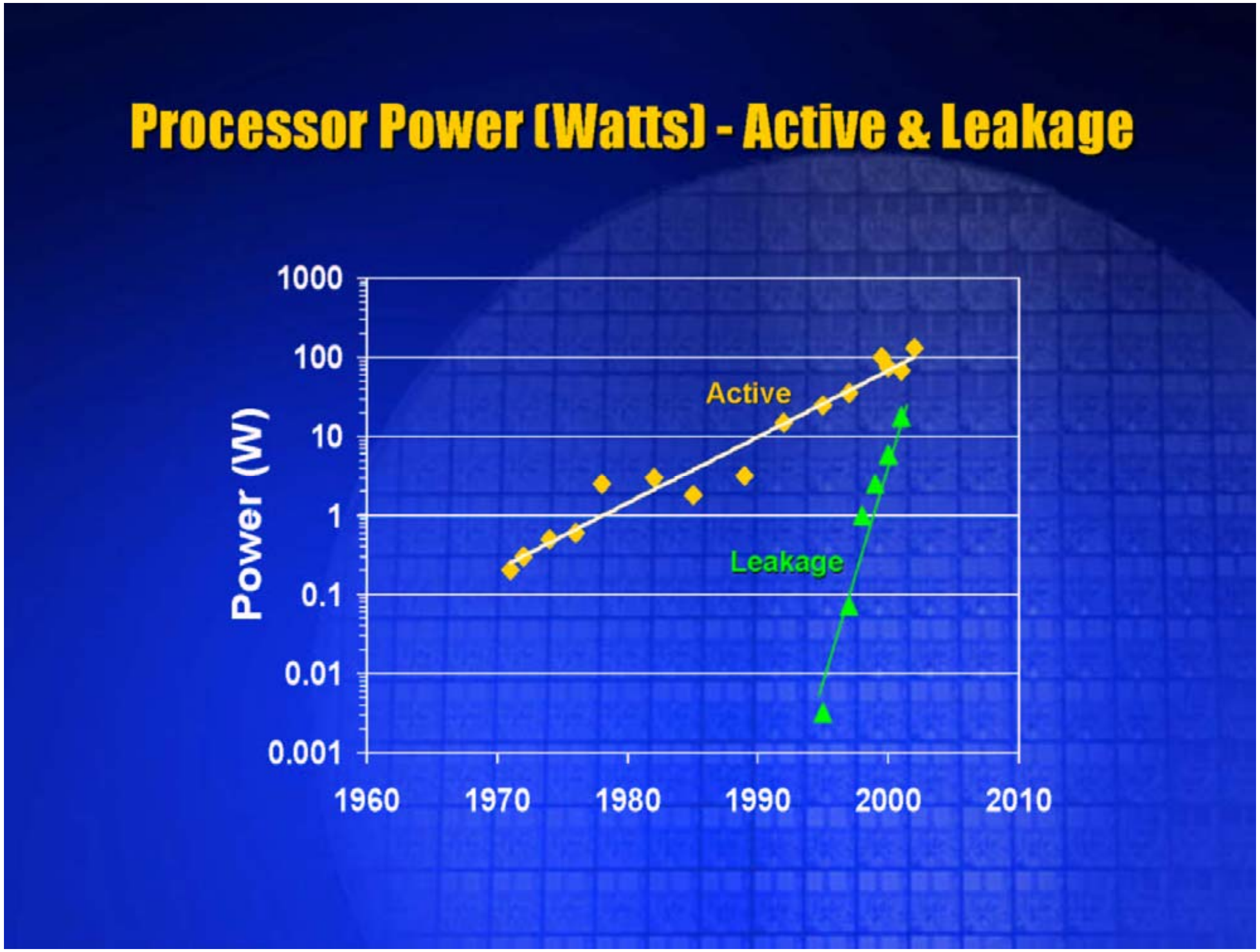
(6) Power Dissipation

→ Although CMOS ideally has no steady state power dissipation, power is dissipated during switching.

→ As clock speed and device densities increase, power dissipation increases

→ Steady state leakage power is also increasing due to gate leakage current and leakage to substrate

→ Gate leakage is minimized with high k dielectrics; substrate leakage is minimized with silicon-on-insulator



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